OPERATIONS MANUAL
EBC-C3PLUS

NOTE: *This manual has been designed and created for use as part of the WinSystems Technical Manuals CD and/or the WinSystems website. If this manual or any portion of the manual is downloaded, copied or emailed, the links to additional information (i.e. software, cable drawings) may be inoperable.*

REVISION HISTORY

P/N 403-0312-000B

ECO Number	Date Code	Rev Level
ORIGINATED	030826	B
03-63	031024	C
04-11	040128	C1
04-12	040130	C2
04-18	040226	C3
04-49	040810	C4
07-04	070208	D
07-137, 07-166	080109	D1
08-66	080509	D2

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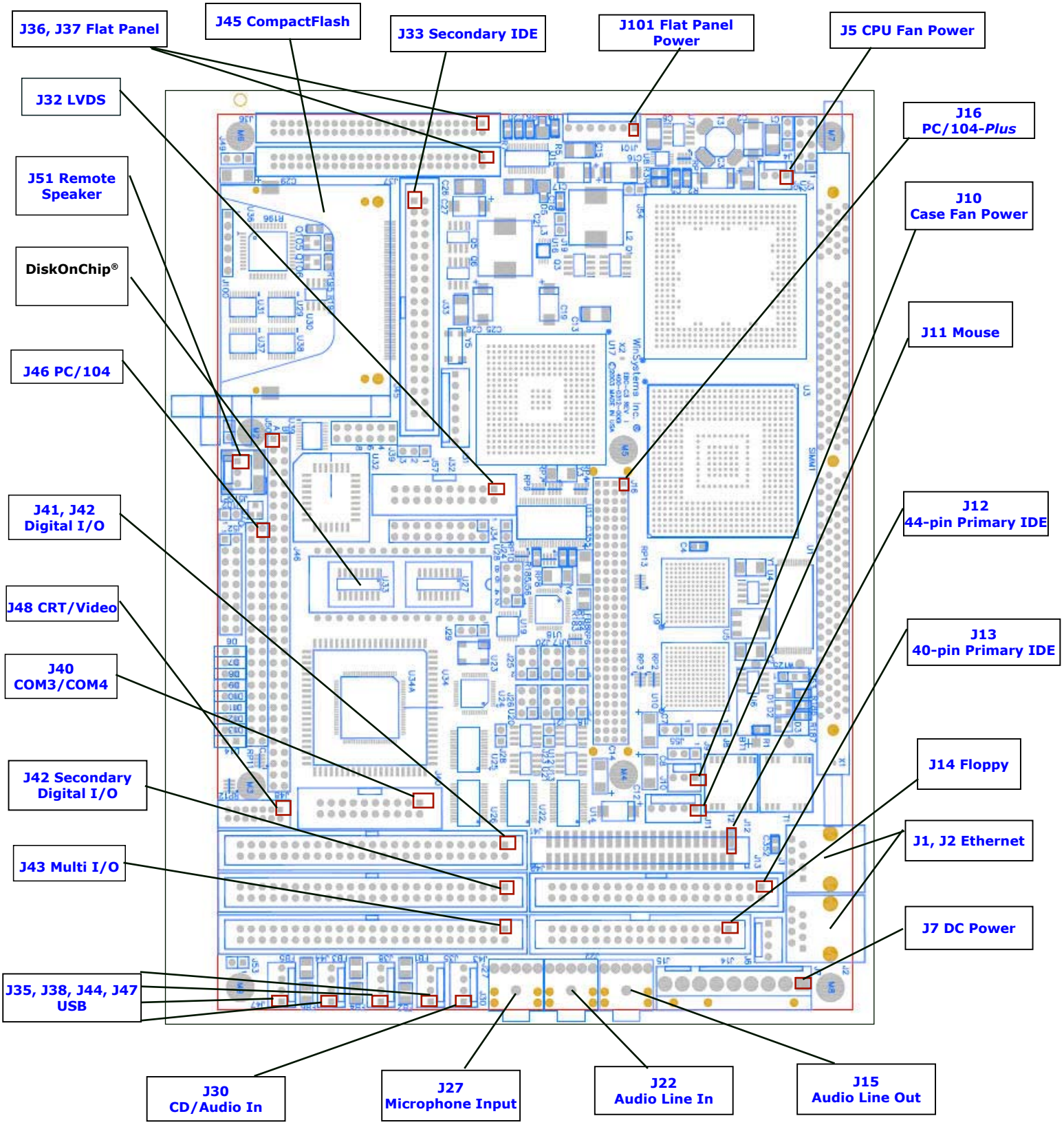
Visual Index – Quick Reference

Top View - Connectors

For the convenience of the user, a copy of the Visual Index has been provided with direct links to connector and jumper configuration data.



NOTE: The reference line to each component part has been drawn to Pin 1, where applicable. Pin 1 is also highlighted with a red square, where applicable.

Visual Index – Quick Reference

Top View - Jumpers

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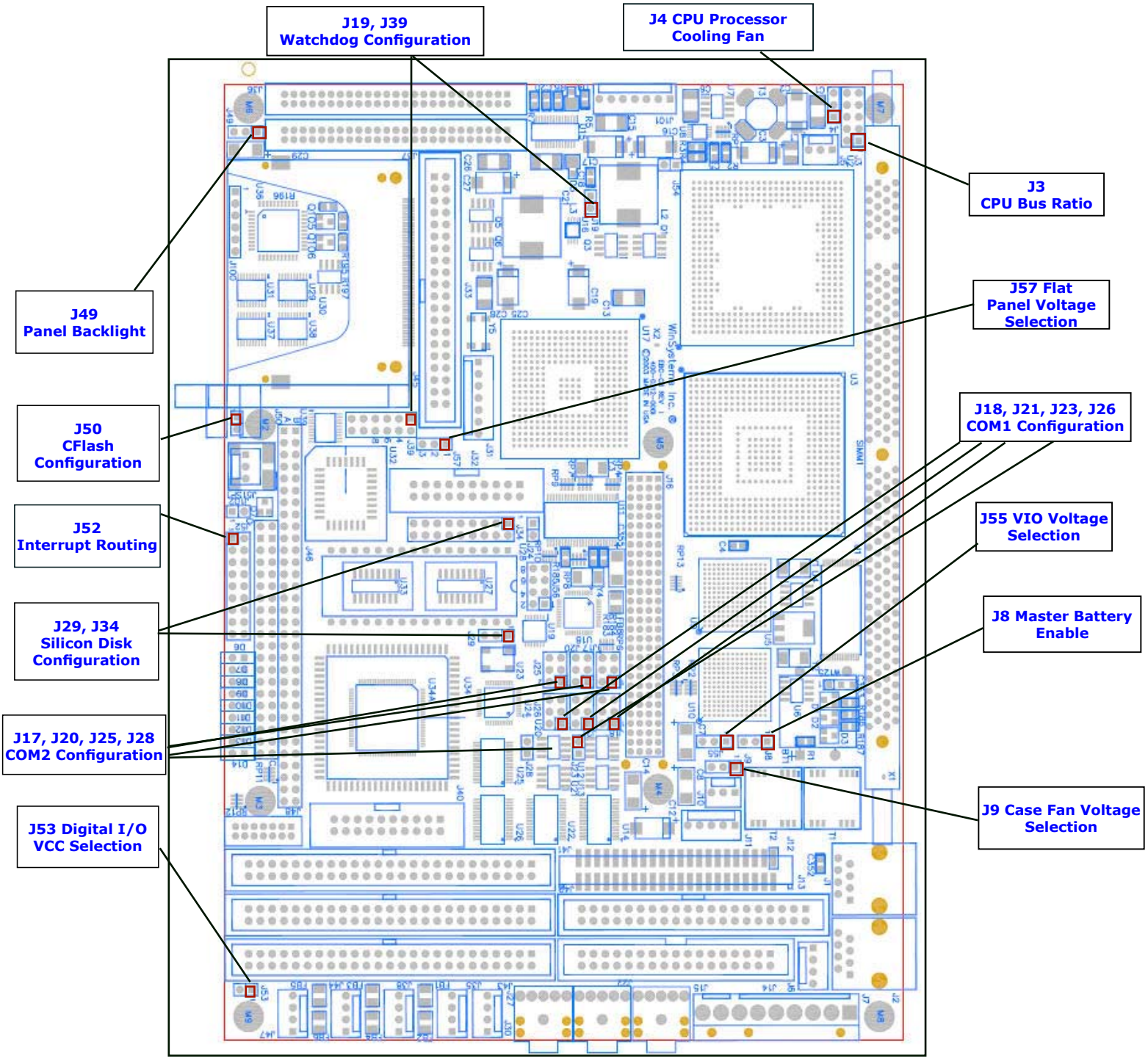


NOTE: The reference line to each component part has been drawn to Pin 1, where applicable. Pin 1 is also highlighted with a red square, where applicable.

Introduction

This manual is intended to provide the necessary information regarding configuration and usage of the EBC-C3PLUS board. WinSystems maintains a Technical Support Group to help answer questions regarding usage or programming of the board. For answers to questions not adequately addressed in this manual, contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

General Information

Features

Processor
- VIA Eden™ 733 MHz C3
- VIA Eden™ 1 GHz C3

Operating Systems Supported
- DOS, Linux, Windows CE, XP, XP Embedded, x86 RTOS

Memory
- Up to 512 MB of 168-pin DIMM PC133 SDRAM (Socketed)

Video
- Up to 1920x1440 resolution
- Up to 36-bits/pixel color panel support
- LVDS Supported

Ethernet
- Intel 82551ER 10/100 Mbps controller

Digital I/O
- 48 Bidirectional lines (WS16C48)

Serial I/O
- Four (4) serial ports (2-RS-232, 2-RS-232/422/485)

Line Printer Port
- EPP/ECP supported

USB
- Four (4) USB 1.1 ports

Interrupts
- Two (2) interrupt controllers
- Seven (7) DMA channels

Watchdog Timer
- Up to 120 second reset

Solid State Devices
- SRAM (up to 512 KB), EPROM (up to 1 MB), DiskOnChip®, CompactFlash

CompactFlash
- Types I & II supported

IDE
- Two (2) IDE ports

Floppy Drive
- Two (2) 3.5” drives supported

Power
- +5V @ 3.3A required

Industrial Operating Temperature Range
- -40°C to 60°C: 1 GHz C3
- -40°C to 85°C: 733 MHz C3

Form Factor
- EBX-compliant
- 5.75” x 8.00” (147 mm x 203 mm)

Additional Specifications
- PC/104 and PC/104-*Plus* expansion connectors
- Phoenix BIOS
- Backlight power supported
- Real-time clock
- Three (3) 16-bit timers
- Simultaneous CRT and LVDS flat panel supported
- Activity status LEDs on-board
- AC97 Support
- AT Keyboard Supported
- PS/2 Mouse Supported

General Description

The EBC-C3PLUS is a full-featured, high-performance, EBX-compliant single board computer (SBC) based upon the VIA C3 processor. These processors have extremely low power dissipation that allows fanless operation, thereby making it ideal for industrial applications. The board is configured with a 1 GHz or a 733 MHz MMX-compatible CPU with up to 512 MB of PC133 SDRAM, plus a CompactFlash socket. The EBC-C3PLUS also has two 10/100 ethernet controllers, USB, video with 3D Now support, four serial channels, 48 digital I/O lines, and the standard AT peripheral feature set. The board measures only 5.75” x 8.0” (147 mm x 203 mm) and is EBX-compliant. It supports expansion with the PC/104 or PC/104-*Plus* connectors or with USB. The board does not require a fan and will operate over an industrial temperature range of -40°C to +85°C, making it ideal for rugged applications requiring an embedded PC. Its x86 PC software compatibility assures a wide range of tools to aid in your applications program development and checkout.

Functional Capability

System Processor

The EBC-C3PLUS is based upon the VIA Technologies' Eden Embedded System Platform Processor architecture. It is manufactured with 0.15/.013µ technology to give high-performance and low power dissipation. The board ships with a 733 MHz or 1 GHz MMX-compatible processor with a 133 MHz front side bus. The CPU includes two, 4-way 64 KB Level 1 cache plus a unified 64 KB Level 2 cache. The CPU and supporting chips are x86 compatible.

A separate 80-bit FPU executes x86 floating point instructions in parallel with integer instructions. The CPU also includes a separate execution unit for MMX instructions.

System Controllers

The VIA VT8606 Twister-T™ is the Northbridge that provides control of the SDRAM and implements the PCI (rev. 2.2) bus controller. PCI is used for on-board peripherals and for the PC/104-*Plus* bus. The VT8606 also integrates the Savage4 graphics core for video. CRTs and LCDs are supported with resolutions up to 1920x1440 with 64 KB colors.

The VIA VT82C6868 Southbridge provides many I/O features and the PC/104 bus controller. It contains the EIDE interface, floppy disk controller, USB root hub, four serial ports, two COM channels, LPT, mouse and keyboard interfaces, plus the AC97 audio controller.

Ethernet Controller

Visual Index

The 82551ER is part of Intel's second generation family of fully integrated 10Base-T/100Base-T LAN solutions. The 82551ER consists of both the Media Access Controller (MAC) and the physical layer (PHY) combined into a single component solution.

The 82551ER is a 32-bit PCI controller that features enhanced scatter/gather bus mastering capabilities which enables it to perform high-speed data transfers over the PCI bus. The 82551ER bus master capabilities enable the component to process high level commands and perform multiple operations, off-loading communications tasks from the system CPU. Two large transmit and receive FIFOS of 3 KB each help prevent data underruns and overruns, allowing the 82551ER to transmit data with minimum interframe spacing (IFS).

The 82551ER can operate in either full-duplex of half-duplex mode. In full-duplex mode, the 82551ER adheres to the IEEE 802.3x Flow Control specification. Half-duplex performance is enhanced by a proprietary condition reduction mechanism.

The 82551ER includes a simple PHY interface to the wire transformer at rates of 10Base-T and 100Base-T, and auto-negotiation for speed, duplex, and flow control. The 82551ER also includes an interface to a serial EEPROM. The EEPROM provides power-on initialization for hardware and software configuration parameters. The 82551ER is 100% PnP compatible and is configured through this interface. There are two ethernet connections on the EBC-C3PLUS. They are provided via the RJ-45 connectors at **J1** (primary) and **J2** (secondary).

There are six ethernet status LEDs at **D8**, **D9**, **D10**, **D11**, **D12** and **D13**. The color and function of each is shown in the following table.

D8	**(GREEN)**	**Ethernet Activity Primary**
D9	**(YELLOW)**	**Link Active Primary**
D10	**(RED)**	**Speed Indication, lit = 100BASE-T Primary**
D11	**(GREEN)**	**Ethernet Activity Secondary**
D12	**(YELLOW)**	**Link Active Secondary**
D13	**(RED)**	**Speed Indication, lit = 100Base-T Secondary**

CPU Clock/Bus Ratio Multiplier

Visual Index

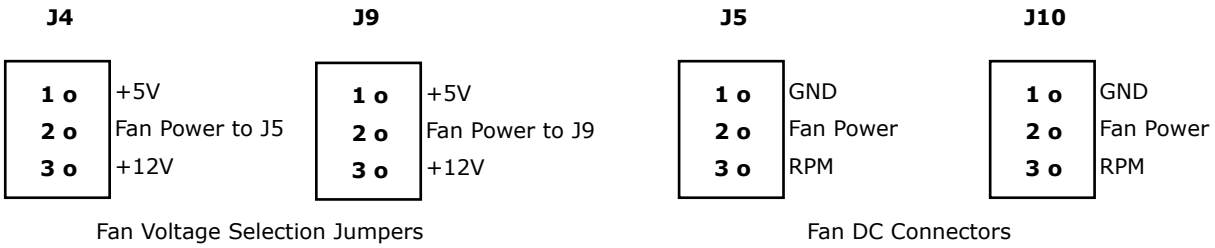
Hardware strapping options for setting the processor's internal clock multiplier is accomplished by jumpering **J3** pins 1-10. This section is for **REFERENCE ONLY**. EBC-C3PLUS CPUs are factory set for the processor installed. Any reconfiguring of this jumper could result in overclocking of the CPU, causing premature failure, and voiding of the warranty.

Bus Ratio	1 - 2	3 - 4	5 - 6	7 - 8	9 - 10
14.5X	open	open	open	open	open
Reserved	1 - 2	open	open	open	open
15.5X	open	3 - 4	open	open	open
Reserved	1 - 2	3 - 4	open	open	open
14.0X	open	open	5 - 6	open	open
16.0X	1 - 2	open	5 - 6	open	open
15.0X	open	3 - 4	5 - 6	open	open
13.0X	1 - 2	3 - 4	5 - 6	open	open
10.5X	open	open	open	7 - 8	open
12.5X	1 - 2	open	open	7 - 8	open
11.5X	open	3 - 4	open	7 - 8	open
13.5X	1 - 2	3 - 4	open	7 - 8	open
Reserved	open	open	5 - 6	7 - 8	open
12.0X	1 - 2	open	5 - 6	7 - 8	open
11.0X	open	3 - 4	5 - 6	7 - 8	open
Reserved	1 - 2	3 - 4	5 - 6	7 - 8	open
6.5X	open	open	open	open	9 - 10
8.5X	1 - 2	open	open	open	9 - 10
7.5X	open	3 - 4	open	open	9 - 10
12.0X	1 - 2	3 - 4	open	open	9 - 10
6.0X	open	open	5 - 6	open	9 - 10
8.0X	1 - 2	open	5 - 6	open	9 - 10
7.0X	open	3 - 4	5 - 6	open	9 - 10
5.0X	1 - 2	3 - 4	5 - 6	open	9 - 10
9.5X	open	open	open	7 - 8	9 - 10
4.5X	1 - 2	open	open	7 - 8	9 - 10
3.5X	open	3 - 4	open	7 - 8	9 - 10
5.5X	1 - 2	3 - 4	open	7 - 8	9 - 10
10.0X	open	open	5 - 6	7 - 8	9 - 10
4.0X	1 - 2	open	5 - 6	7 - 8	9 - 10
3.0X	open	3 - 4	5 - 6	7 - 8	9 - 10
9.0X	1 - 2	3 - 4	5 - 6	7 - 8	9 - 10

Fan Speed / Power

Visual Index

There are connectors for two optional fans available on the EBC-C3PLUS. Fan number one is for the CPU processor and fan number two is the case fan available for application specific purposes. Connection to the fan is made using the jumper headers at **J5** and **J10**. Voltage for the fans is selected using the jumpers at **J4** and **J9**, respectively. There are two fan voltages available, +5V and +12V. The pinout for the fan connectors and the jumpering to select proper voltage for each fan is shown below.



Fan Voltage Selection Jumpers

Fan DC Connectors

Power and Reset Interface

Visual Index

Power is applied to the EBC-C3PLUS via the connector at **J7** (Molex part number 26-60-7091). The pin definitions for **J7** are given below. An optional reset push-button (normally OPEN) may also be routed into **J7** if desired. Momentary closure to ground forces a hardware reset.

J7

9 o	PB Reset
8 o	-12V
7 o	+5V
6 o	GND
5 o	+3.3V (**only connects to the PC/104-Plus connector**)
4 o	+12V
3 o	GND
2 o	GND
1 o	+5V

Mouse Interface

Visual Index

A PS/2 mouse may be attached via the connector at **J11**. An adapter cable, CBL-225-1, is available from WinSystems to adapt to a conventional PS/2 mouse connector. The pinout for **J11** is shown here for reference.

J11

1 o	MSDATA
2 o	N/C
3 o	GND
4 o	VCC
5 o	MSCLK

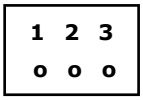
Real-Time Clock/Calendar

Visual Index

The EBC-C3PLUS contains an on-board clock/calendar within the VIA Technologies VT82C686B chip. This clock is fully compatible with the MC146818A used in the original PC-AT computers. This clock has a number of features including periodic and alarm interrupt capabilities. In addition to the time and date keeping functions, the system configuration is kept within the CMOS RAM contained in the clock. This RAM holds all of the setup information regarding hard and floppy disk types, video type, shadowing, wait states, etc. Refer to the BIOS Supplemental for CMOS RAM configuration.

It may become necessary at some time to make the CMOS RAM forget its current configuration and to start fresh with factory defaults. This may be accomplished by removing power from the board. Next, remove the jumper from pins 1-2 on **J8** and place on pins 2-3 for 10 seconds. Replace the jumper on **J8** pins 1-2, power-up, and reconfigure the CMOS settings as desired.

J8



Primary IDE Interface

Visual Index

The EBC-C3PLUS supports standard IDE fixed disks through the I/O connectors at **J13** (40-pin primary) or **J12** (44-pin primary). A red activity LED is present at **D6** for the primary hard drive controller. The pin definitions for **J12** and **J13** are shown below.

J12

Reset*	1 o o 2	GND
D7	3 o o 4	D8
D6	5 o o 6	D9
D5	7 o o 8	D10
D4	9 o o 10	D11
D3	11 o o 12	D12
D2	13 o o 14	D13
D1	15 o o 16	D14
D0	17 o o 18	D15
GND	19 o o 20	N/C
DRQ	21 o o 22	GND
IOW	23 o o 24	GND
IOR	25 o o 26	GND
RDY	27 o o 28	N/C
DACK	29 o o 30	GND
IRQ	31 o o 32	IOCS16*
A1	33 o o 34	66/100 MHz
A0	35 o o 36	A2
HDSC0	37 o o 38	HDSC1
LED	39 o o 40	GND
VCC	41 o o 42	VCC
GND	43 o o 44	GND

J13

Reset*	1 o o 2	GND
D7	3 o o 4	D8
D6	5 o o 6	D9
D5	7 o o 8	D10
D4	9 o o 10	D11
D3	11 o o 12	D12
D2	13 o o 14	D13
D1	15 o o 16	D14
D0	17 o o 18	D15
GND	19 o o 20	N/C
DRQ	21 o o 22	GND
IOW	23 o o 24	GND
IOR	25 o o 26	GND
RDY	27 o o 28	N/C
DACK	29 o o 30	GND
IRQ	31 o o 32	N/C
A1	33 o o 34	66/100 MHz
A0	35 o o 36	A2
HDSC0	37 o o 38	HDSC1
LED	39 o o 40	GND

CompactFlash

The EBC-C3PLUS supports standard IDE fixed disks and CompactFlash modules through the I/O connector at **J33** (40-pin secondary) and CompactFlash modules through the CompactFlash connector at **J45**. The EBC-C3PLUS will only support CompactFlash modules with TrueIDE support. A red activity LED is present at **D7** for both secondary hard drive connectors respectively. The pin definitions for **J33** and **J45** are:

J33

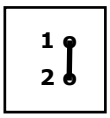
Reset*	**1 o o 2**	GND
D7	**3 o o 4**	D8
D6	**5 o o 6**	D9
D5	**7 o o 8**	D10
D4	**9 o o 10**	D11
D3	**11 o o 12**	D12
D2	**13 o o 14**	D13
D1	**15 o o 16**	D14
D0	**17 o o 18**	D15
GND	**19 o o 20**	N/C
DRQ	**21 o o 22**	GND
IOW	**23 o o 24**	GND
IOR	**25 o o 26**	GND
RDY	**27 o o 28**	N/C
DACK	**29 o o 30**	GND
IRQ	**31 o o 32**	N/C
A1	**33 o o 34**	SPDSEL
A0	**35 o o 36**	A2
CS1	**37 o o 38**	CS3
LED	**39 o o 40**	GND

J45

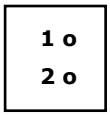
GND	**1 o o 2**	D3
D4	**3 o o 4**	D5
D6	**5 o o 6**	D7
HDSC0	**7 o o 8**	GND
GND	**9 o o 10**	GND
GND	**11 o o 12**	GND
CFVCC	**13 o o 14**	GND
GND	**15 o o 16**	GND
GND	**17 o o 18**	A2
A1	**19 o o 20**	A0
D0	**21 o o 22**	D1
D2	**23 o o 24**	N/C
CFEN	**25 o o 26**	CFEN
D11	**27 o o 28**	D12
D13	**29 o o 30**	D14
D15	**31 o o 32**	HDCS1
GND	**33 o o 34**	IOR
IOW	**35 o o 36**	VCC3.3
IRQ	**37 o o 38**	CFVCC
Slave/Master	**39 o o 40**	N/C
Reset*	**41 o o 42**	RDY
N/C	**43 o o 44**	VCC3.3
LED	**45 o o 46**	66/100MHz
D8	**47 o o 48**	D9
D10	**49 o o 50**	GND

When using a CompactFlash device, Master/Slave mode selection can be accomplished by jumpering **J50**, shown below.

J50



Master Mode



Slave Mode

Rotational Disk Support

Visual Index

The EBC-C3PLUS supports up to two standard 3.5” or 5.25” PC-compatible floppy disk drives. The drives are connected via the I/O connector at **J14**. Note the interconnect cable to the drives is a standard floppy I/O cable used on desktop PCs. The cable must have the twisted section prior to the drive A position. The pin definition for the **J14** connector is below:

J14

GND	**1 o o 2**	RPM/LC
GND	**3 o o 4**	N/C
GND	**5 o o 6**	N/C
GND	**7 o o 8**	INDEX
GND	**9 o o 10**	MTR0
GND	**11 o o 12**	DRV1
GND	**13 o o 14**	DRV0
GND	**15 o o 16**	MTR1
GND	**17 o o 18**	DIR
GND	**19 o o 20**	STEP
GND	**21 o o 22**	WDATA
GND	**23 o o 24**	WGATE
GND	**25 o o 26**	TKR0
GND	**27 o o 28**	WPRT
GND	**29 o o 30**	RDATA
GND	**31 o o 32**	HDSEL
GND	**33 o o 34**	DSKCHG

Memory

The EBC-C3PLUS can support a maximum of up to 512 MB of RAM with the SODIMM socket located on the board at **SIMM1**.

Qualified SODIMMS are available directly from WinSystems. WinSystems cannot warrant the operation of systems using nonqualified SODIMM modules.

The RAM can be user supplied but must meet the following criteria:

64, 128, 256, 512 MB of 168-Pin DIMM PC133 SDRAM with gold fingers

DIMM modules should be a minimum speed of PC133 and x64. Either ECC or nonECC parts may be used. A single DIMM socket is provided which can support SDRAM sized from 64 MB to 512 MB.

Installation is accomplished by inserting the module into the connector at approximately a 30 degree angle. Press firmly to fully seat the module into the connector and then press the module downward to snap it into the retaining clamps.

Removal is accomplished by gently pulling outward on the retaining clamps until the module springs up to the appropriate removal angle.

PC/104 Bus Interface

The EBC-C3PLUS supports the PC/104 bus which is basically the original ISA bus with the 16-bit extensions. A vast array of PC/104 stack on modules are available from WinSystems and other PC/104 suppliers. The PC/104 bus connector (**J46**) pin definitions are provided here for reference. Refer to the PC/104 Bus Specification for specific signal and mechanical specifications.

Visual Index

GND	**D0 o o C0**	GND
MEMCS16#	**D1 o o C1**	SBHE#
IOCS16#	**D2 o o C2**	LA23
IRQ10	**D3 o o C3**	LA22
IRQ11	**D4 o o C4**	LA21
IRQ12	**D5 o o C5**	LA20
IRQ15	**D6 o o C6**	LA19
IRQ14	**D7 o o C7**	LA18
DACK0#	**D8 o o C8**	LA17
DRQ0	**D9 o o C9**	MEMR#
DACK5#	**D10 o o C10**	MEMW#
DRQ5	**D11 o o C11**	SD8
DACK6#	**D12 o o C12**	SD9
DRQ6	**D13 o o C13**	SD10
DACK7#	**D14 o o C14**	SD11
DRQ7	**D15 o o C15**	SD12
+5V	**D16 o o C16**	SD13
MASTER#	**D17 o o C17**	SD14
GND	**D18 o o C18**	SD15
GND	**D19 o o C19**	KEY

= Active Low Signal

IOCHK#	**A1 o o B1**	GND
SD7	**A2 o o B2**	RESET
SD6	**A3 o o B2**	+5V
SD5	**A4 o o B4**	IRQ9
SD4	**A5 o o B5**	-5V
SD3	**A6 o o B6**	DRQ2
SD2	**A7 o o B7**	-12V
SD1	**A8 o o B8**	SRDY#
SD0	**A9 o o B9**	+12V
IOCHRDY	**A10 o o B10**	KEY
AEN	**A11 o o B11**	SMEMW#
SA19	**A12 o o B12**	SMEMR#
SA18	**A13 o o B13**	IOW#
SA17	**A14 o o B14**	IOR#
SA16	**A15 o o B15**	DACK3#
SA15	**A16 o o B16**	DRQ3
SA14	**A17 o o B17**	DACK1#
SA13	**A18 o o B18**	DRQ1
SA12	**A19 o o B19**	REFRESH#
SA11	**A20 o o B20**	BCLK
SA10	**A21 o o B21**	IRQ7
SA9	**A22 o o B22**	IRQ6
SA8	**A23 o o B23**	IRQ5
SA7	**A24 o o B24**	IRQ4
SA6	**A25 o o B25**	IRQ3
SA5	**A26 o o B26**	DACK2#
SA4	**A27 o o B27**	TC
SA3	**A28 o o B28**	BALE
SA2	**A29 o o B29**	+5V
SA1	**A30 o o B30**	OSC
SA0	**A31 o o B31**	GND
GND	**A32 o o B32**	GND

NOTES:

1. Rows C and D are not required on 8-bit modules.
2. B10 and C19 are key locations. WinSystems uses key pins as connections to GND.
3. Signal timing and function are as specified in ISA specification.
4. Signal source/sink current differ from ISA values.

PC/104-*Plus* Bus Interface

Visual Index

The EBC-C3PLUS also supports peripheral expansion using the PC/104-*Plus* connector at **J16**. Up to three PC/104-*Plus* modules may be stacked onto the EBC-C3PLUS. PC/104-*Plus* modules should be attached and configured beginning at slot 1. The PC/104-*Plus* bus pin definitions are shown here for reference purposes only. Refer to the PC/104-*Plus* Bus Specification for signal definitions, timing and mechanical details.

Pin	A	B	C	D
1	GND	RESERVED	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	RESERVED	PAR
10	GND	PERR#	+3.3V	RESERVED
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O
24	GND	REQ2#	+5V	GNT0#
25	GNT1#	VI/O	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD#	+5V	RST#
29	+12V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND

Note: 1. The shaded area denotes power or ground signals.

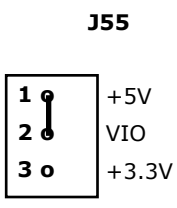
PC/104-*Plus* VIO Voltage Selection

Visual Index

PC/104-*Plus* VIO voltage is selected by jumpering **J55**.

J55 jumpered 1-2 supports +5V (default, shown)

J55 jumpered 2-3 supports +3.3V



Video Interface

Visual Index

The EBC-C3PLUS uses the VT8606 integrated Savage4 SVGA controller. It supports standard CRT displays as well as a variety of liquid crystal displays (LCD) also known as *flat panels*. The CRT interface is located at **J48**. LCDs require optional Flat Panel Adapter (FPA) kits. The Savage4 controller supports standard and SuperVGA as well as color and monochrome or LVDS connections via **J32**, with 8, 9, 12, 15, 16, 18, 24 and 36-bit interfaces.

WinSystems provides flat panel support through a series of Flat Panel Adapter (FPA) kits. Contact your WinSystems' Applications Engineer for the most current list of available FPAs and supported panels. **This manual does not attempt to provide any information about how to connect to specific LCDs.** Attempted connection to any flat panel not directly supported by a WinSystems' FPA module is at the user's risk. Extreme care should be exercised to avoid damaging or destroying the panel.

HAZARD WARNING: LCD panels can require a high voltage for the panel backlight. This high-frequency voltage can exceed 1000 volts and can present a shock hazard. Care should be taken when wiring and handling the inverter output. To avoid danger of shock and to avoid damaging fragile and expensive panels, make all connection changes with power removed.

NOTE: J49 must be jumpered 1-2 for an active low backlight inverter, and 2-3 for an active high backlight inverter.

J49

1 o	
2 o	
3 o	

1-2 for Active Low
2-3 for Active High

CRT Output Connection

Visual Index

Video output to a standard VGA monitor is made via the connector at **J48**. And adapter cable, part number CBL-234-1, is available from WinSystems to adapt from **J48** to the standard DB15 VGA connector. The pin definitions for the **J48** connector are:

J48

RED	**1 o o 2**	GND
GREEN	**3 o o 4**	GND
BLUE	**5 o o 6**	GND
HSYNC	**7 o o 8**	GND
VSYNC	**9 o o 10**	GND
DDCDATA	**11 o o 12**	GND
DDCCLK	**13 o o 14**	VCC

Panel Backlight Connection

Visual Index

Panel backlight connection is made via the connector at **J101**. The pinout for **J101** is shown here for reference.

J101

+12	**1 o**
+12	**2 o**
GND	**3 o**
GND	**4 o**
ENBKL	**5 o**
VCC	**6 o**
VCC	**7 o**

LVDS Connector

Visual Index

There are two LVDS channels (Low Voltage Differential Signals) available on the EBC-C3PLUS. Connection is made via the connector at **J32**. Channel one connection is made through pins 1-10 and channel two connection is made through pins 11-20. Pinout for the connector is:

J32

Channel 1	D0-	**1 o o 2**	D0+	Channel 1
	D1-	**3 o o 4**	D1+	
	D2-	**5 o o 6**	D2+	
	GND	**7 o o 8**	CLK+	
	CLK-	**9 o o 10**	VCC	
Channel 2	D0-	**11 o o 12**	D0+	Channel 2
	GND	**13 o o 14**	D1+	
	D1-	**15 o o 16**	D2+	
	D2-	**17 o o 18**	CLK+	
	CLK	**19 o o 20**	VCC	

Flat Panel Output Connection

Visual Index

Connection to all nonLVDS flat panels is made via the two 50-pin connectors at **J36** and **J37**. These connectors are cabled to the appropriate FPA (Flat Panel Adapter) module which then breaks out the necessary cabling for attachment to the panel itself. The FPA module also supplies any special controls that may be needed for the panel. Refer to the FPA documentation for specific hookup instructions. The pin definitions for **J36** and **J37** are shown here:

J36

FP12	**1 o o 2**	GND
FP13	**3 o o 4**	GND
FP14	**5 o o 6**	GND
FP15	**7 o o 8**	GND
FP16	**9 o o 10**	GND
FP17	**11 o o 12**	GND
FP18	**13 o o 14**	GND
FP19	**15 o o 16**	GND
FP20	**17 o o 18**	GND
FP21	**19 o o 20**	GND
FP22	**21 o o 22**	GND
FP23	**23 o o 24**	GND
FP24	**25 o o 26**	GND
FP25	**27 o o 28**	GND
FP26	**29 o o 30**	GND
FP27	**31 o o 32**	GND
FP28	**33 o o 34**	GND
FP29	**35 o o 36**	GND
FP30	**37 o o 38**	GND
FP31	**39 o o 40**	GND
FP32	**41 o o 42**	GND
FP33	**43 o o 44**	GND
FP34	**45 o o 46**	GND
FP35	**47 o o 48**	GND
SWVCC	**49 o o 50**	GND

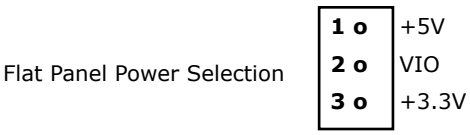
J37

SW0	**1 o o 2**	SW1
SW2	**3 o o 4**	SW3
FP0	**5 o o 6**	GND
FP1	**7 o o 8**	GND
FP2	**9 o o 10**	GND
FP3	**11 o o 12**	GND
FP4	**13 o o 14**	GND
FP5	**15 o o 16**	GND
FP6	**17 o o 18**	GND
FP7	**19 o o 20**	GND
FP8	**21 o o 22**	GND
FP9	**23 o o 24**	GND
FP10	**25 o o 26**	GND
FP11	**27 o o 28**	GND
PCSHCLK	**29 o o 30**	GND
PCFLM	**31 o o 32**	GND
PCLP	**33 o o 34**	GND
PCM	**35 o o 36**	GND
PHSYNC	**37 o o 38**	GND
PVSYNC	**39 o o 40**	GND
ENVCC	**41 o o 42**	GND
ENBKL	**43 o o 44**	GND
ENVEE	**45 o o 46**	-12V
+12V	**47 o o 48**	+12V
SWVCC	**49 o o 50**	SWVCC

Flat Panel Power Selection

Visual Index

Panel power is selected by jumpering **J57**. There are two voltages available on the EBC-C3PLUS, +5V by jumpering **J57** 1-2, +3V by jumpering **J57** 2-3. Power is supplied to pins 49 and 50 of both **J36** and **J37**.

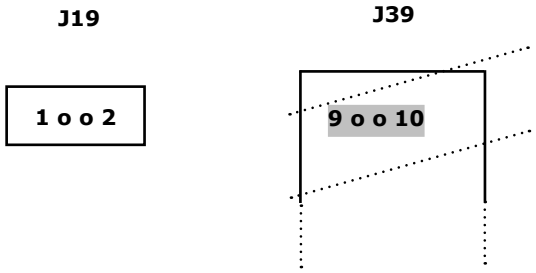


Watchdog Timer

Visual Index

The EBC-C3PLUS board features a power-on voltage detect, and power-down/power brownout reset circuit to protect memory and I/O from faulty CPU operation during periods of illegal voltage levels. This supervisor circuitry also features a watchdog timer which can be used to guard against software lockups. An internal timer with a period of 1.5s with **J19** open, or 200s with **J19** closed, will reset the CPU if the watchdog has not been serviced within the allotted time. The watchdog timer power-up is disabled if **J39** pins 9-10 are closed, and must be enabled in software before timing will begin. Enabling is accomplished by writing a **1** to I/O port 1EEH. Writing a **0** to I/O port 1EEH will disable the watchdog. After enabling, petting may be accomplished by writing any value to I/O port 1EFH within the timeout period. If **J39** pins 9-10 are not jumpered, the watchdog is always enabled and petting must begin at once.

NOTE: It is recommended that the long timeout (200s) be used with the watchdog enabled when trying to boot any operating system.



Digital I/O

The EBC-C3PLUS utilizes the WinSystems WS16C48 ASIC high-density I/O chip mapped at a base address of 120H. The first 24 lines are capable of fully latched event sensing with sense polarity being software programmable. Two, 50-pin connectors allow for easy mating with industry standard I/O racks.

J41

Port 2 Bit 7	**1 o o 2**	GND
Port 2 Bit 6	**3 o o 4**	GND
Port 2 Bit 5	**5 o o 6**	GND
Port 2 Bit 4	**7 o o 8**	GND
Port 2 Bit 3	**9 o o 10**	GND
Port 2 Bit 2	**11 o o 12**	GND
Port 2 Bit 1	**13 o o 14**	GND
Port 2 Bit 0	**15 o o 16**	GND
Port 1 Bit 7	**17 o o 18**	GND
Port 1 Bit 6	**19 o o 20**	GND
Port 1 Bit 5	**21 o o 22**	GND
Port 1 Bit 4	**23 o o 24**	GND
Port 1 Bit 3	**25 o o 26**	GND
Port 1 Bit 2	**27 o o 28**	GND
Port 1 Bit 1	**29 o o 30**	GND
Port 1 Bit 0	**31 o o 32**	GND
Port 0 Bit 7	**33 o o 34**	GND
Port 0 Bit 6	**35 o o 36**	GND
Port 0 Bit 5	**37 o o 38**	GND
Port 0 Bit 4	**39 o o 40**	GND
Port 0 Bit 3	**41 o o 42**	GND
Port 0 Bit 2	**43 o o 44**	GND
Port 0 Bit 1	**45 o o 46**	GND
Port 0 Bit 0	**47 o o 48**	GND
+5V	**49 o o 50**	GND

J42

Port 5 Bit 7	**1 o o 2**	SW1
Port 5 Bit 6	**3 o o 4**	SW3
Port 5 Bit 5	**5 o o 6**	GND
Port 5 Bit 4	**7 o o 8**	GND
Port 5 Bit 3	**9 o o 10**	GND
Port 5 Bit 2	**11 o o 12**	GND
Port 5 Bit 1	**13 o o 14**	GND
Port 5 Bit 0	**15 o o 16**	GND
Port 4 Bit 7	**17 o o 18**	GND
Port 4 Bit 6	**19 o o 20**	GND
Port 4 Bit 5	**21 o o 22**	GND
Port 4 Bit 4	**23 o o 24**	GND
Port 4 Bit 3	**25 o o 26**	GND
Port 4 Bit 2	**27 o o 28**	GND
Port 4 Bit 1	**29 o o 30**	GND
Port 4 Bit 0	**31 o o 32**	GND
Port 3 Bit 7	**33 o o 34**	GND
Port 3 Bit 6	**35 o o 36**	GND
Port 3 Bit 5	**37 o o 38**	GND
Port 3 Bit 4	**39 o o 40**	GND
Port 3 Bit 3	**41 o o 42**	GND
Port 3 Bit 2	**43 o o 44**	GND
Port 3 Bit 1	**45 o o 46**	GND
Port 3 Bit 0	**47 o o 48**	GND
+5V	**49 o o 50**	GND

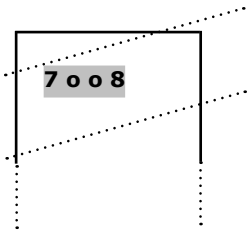
Digital I/O Enable

The parallel features of the EBC-C3PLUS can be enabled or disabled using the jumper block at **J39**, pins 7-8. When **J39** pins 7-8 are jumpered, the digital I/O is enabled at I/O address 120H. When **J39** pins 7-8 are open, the 16 addresses starting at I/O address 120H are free for use by other devices.

7-8 jumpered - the digital I/O is enabled at I/O address 120H

7-8 are open - the 16 addresses starting at I/O address 120H are free for use by other devices

J39

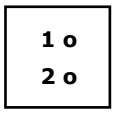


Digital I/O VCC Enable

The I/O connectors can provide +5V to an I/O rack or for miscellaneous purposes by jumpering **J53**. When **J53** is jumpered +5V is provided at pin 49 of both **J41** and **J42**. It is the user's responsibility to limit current to a safe value (less than 400 mA) to avoid damaging the CPU board.

J53

1-2 jumpered - +5V is provided at pin 49 of both J41 and J42



Digital I/O Connector

The 48 lines of digital I/O are terminated through two 50-pin connectors at **J41** and **J42**. The **J41** connector handles I/O Ports 0 through 2 while **J42** handles Ports 3 through 5. The pin definitions for **J41** and **J42** are shown on the previous page.

Software Summary

WS16C48 Register Definitions

The EBC-C3PLUS uses the WinSystems exclusive ASIC device, the WS16C48. This device provides 48 lines of digital I/O. There are 17 unique registers within the WS16C48. The following table summarizes the registers and the text that follows provides details on each of the internal registers.

I/O Address Offset	Page 0	Page 1	Page 2	Page 3
00H	Port 0 I/O	Port 0 I/O	Port 0 I/O	Port 0 I/O
01H	Port 1 I/O	Port 1 I/O	Port 1 I/O	Port 1 I/O
02H	Port 2 I/O	Port 2 I/O	Port 2 I/O	Port 2 I/O
03H	Port 3 I/O	Port 3 I/O	Port 3 I/O	Port 3 I/O
04H	Port 4 I/O	Port 4 I/O	Port 4 I/O	Port 4 I/O
05H	Port 5 I/O	Port 5 I/O	Port 5 I/O	Port 5 I/O
06H	Int_ Pending	Int_ Pending	Int_ Pending	Int_ Pending
07H	Page/Lock	Page/Lock	Page/Lock	Page/Lock
08H	N/A	Pol_0	Enab_0	Int_ID0
09H	N/A	Pol_1	Enab_1	Int_ID1
0AH	N/A	Pol_2	Enab_2	Int_ID2

Register Details

Port 0 through 5 I/O – Each I/O bit in each of the six ports can be individually programmed for input or output. Writing a **0** to a bit position causes the corresponding output pin to go to a high-impedance state (pulled high by external 10 KΩ resistors). This allows it to be used as an input. When used in the input mode, a read reflects the inverted state of the I/O pin, such that a high on the pin will read as a **0** in the register. Writing a **1** to a bit position causes that output pin to sink current (up to 12 mA), effectively pulling it low.

INT_PENDING – This read-only register reflects the combined state of the INT_ID0 through INT_ID2 registers. When any of the lower three bits are set, it indicates that an interrupt is pending on the I/O port corresponding to the bit position(s) that are set. Reading this register allows an Interrupt Service Routine to quickly determine if any interrupts are pending and which I/O port has a pending interrupt.

PAGE/LOCK – This register serves two purposes. The upper two bits select the register page in use as shown here:

D7	D6	Page
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Bits 5-0 allow for locking the I/O ports. A **1** written to the I/O port position will prohibit further writes to the corresponding I/O port.

POL0 - POL2 – These registers are accessible when Page 1 is selected. They allow interrupt polarity selection on a port–by–port and bit-by-bit basis. Writing a **1** to a bit position selects the rising edge detection interrupts while writing a **0** to a bit position selects falling edge detection interrupts.

ENAB0 - ENAB2 – These registers are accessible when Page 2 is selected. They allow for port-by-port and bit-by-bit enabling of the edge detection interrupts. When set to a **1**, the edge detection interrupt is enabled for the corresponding port and bit. When cleared to **0**, the bit's edge detection interrupt is disabled. Note that this register can be used to individually clear a pending interrupt by disabling and reenabling the pending interrupt.

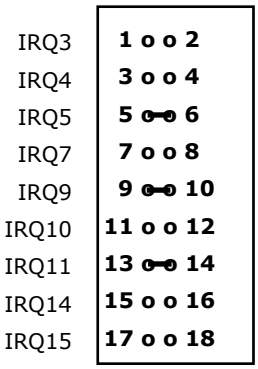
INT_ID0 – INT_ID2 – These registers are accessible when Page 3 is selected. They are used to identify currently pending edge interrupts. A bit when read as a **1** indicates that an edge of the polarity programmed into the corresponding polarity register has been recognized. Note that a write to this register (value ignored) clears ALL of the pending interrupts in this register.

Interrupt Routing

Visual Index

All interrupts are routed to their respective PC/104 bus pins. On-board nonPnP peripherals are routed to their typical usage interrupts using the jumper block at **J52**. This block allows disconnecting or rerouting of the on-board interrupts. The layout and default jumper settings for **J52** are shown below.

J52



Multi-I/O Connector

Visual Index

The I/O to the primary serial channels, the printer port, and keyboard are all terminated via the connector at **J43**. An adapted cable, part number CBL-247-1, is available from WinSystems to adapt to the conventional I/O connectors. The pin definitions for **J43** are:

J43

COM1*	**1 o o 2**	COM1*
COM1*	**3 o o 4**	COM1*
COM1*	**5 o o 6**	COM1*
COM1*	**7 o o 8**	COM1*
COM1*	**9 o o 10**	COM2*
COM2*	**11 o o 12**	COM2*
COM2*	**13 o o 14**	COM2*
COM2*	**15 o o 16**	COM2*
COM2*	**17 o o 18**	COM2*
LPT-STROBE	**19 o o 20**	LPT-AUTOFD
LPT-PD0	**21 o o 22**	LPT-ERROR
LPT-PD1	**23 o o 24**	LPT-INIT
LPT-PD2	**25 o o 26**	LPT-SLCTIN
LPT-PD3	**27 o o 28**	LPT-GND
LPT-PD4	**29 o o 30**	LPT-GND
LPT-PD5	**31 o o 32**	LPT-GND
LPT-PD6	**33 o o 34**	LPT-GND
LPT-PD7	**35 o o 36**	LPT-GND
LPT-ACK	**37 o o 38**	LPT-GND
LPT-BUSY	**39 o o 40**	LPT-GND
LPT-PE	**41 o o 42**	LPT-GND
LPT-SLCT	**43 o o 44**	KEYBD-GND
KEYBD-GND	**45 o o 46**	KEYBD-GND
KEYBD-KDATA	**47 o o 48**	KEYBD-CLK
KEYBD-+5V	**49 o o 50**	KEYBD-+5V

*** NOTE**: Pins 1-9 are used for COM1, pins 10-18 are used for COM2. Pin definitions for use as RS-232, RS-422 or RS-485 are shown in the Serial Interface Section of this manual.

USB

Visual Index

Up to four USB cables may be attached to the EBC-C3PLUS via the connectors at **J35**, **J38**, **J44** and **J47**. An adapter cable, CBL-249-1, is available from WinSystems to adapt to a conventional USB port. The pinout of each of the USB connectors is shown here.

J35

1 o	USBVCC
2 o	USBD0-
3 o	USBD0+
4 o	USBGND

USB1

J38

1 o	USBVCC
2 o	USBD1-
3 o	USBD1+
4 o	USBGND

USB2

J44

1 o	USBVCC
2 o	USBD2-
3 o	USBD2+
4 o	USBGND

USB3

J47

1 o	USBVCC
2 o	USBD3-
3 o	USBD3+
4 o	USBGND

USB4

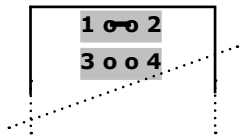
Silicon Disk Configuration

Visual Index

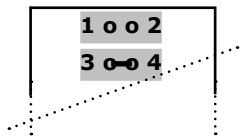
The EBC-C3PLUS supports the use of EPROM, PEROM (Flash), SRAM, and the SanDisk DiskOnChip® (DOC) devices to be used as a Solid State Disk drive. This section documents the required hardware configurations for the various types of devices. The 32-pin JEDEC memory socket at **U28** is used to contain the RAM, ROM, Flash, of DOC device used for the disk. The silicon disk array is memory mapped into a 16 KB hole at a segment specified by jumpering **J34** as shown in the chart titled Silicon Disk Address Selection. An I/O page register is present at 1ECH.

Silicon Disk Mode

There are two basic modes of Silicon Disk operation available on the EBC-C3PLUS. The first uses RAM or ROM (nonbootable disk) and must use USSD.SYS for access. The second mode uses the SanDisk DiskOnChip® device. The mode is controlled via pins 1-2 and 3-4 on jumper block at **J34**.



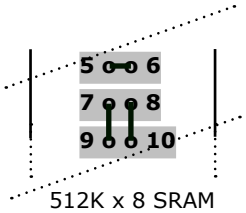
DOC usage



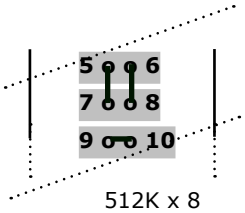
EPROM, SRAM, PEROM usage

Device Type Selection

Before using the Silicon Disk, the proper device type must be selected by properly jumpering **J34**. Jumpering for the supported device types are:



512K x 8 SRAM

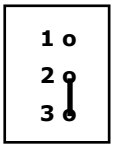


512K x 8
EPROM \ PEROM \ DiskOnChip usage

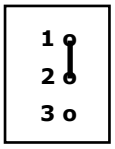
Battery Backup Selection

When using SRAM devices and nonvolatile operation is desired, battery backup can be selected. **J29** provides for selecting battery backed vs. normal operating mode, as shown:

J29



Normal Operation



Battery Backup Selected

NOTE: Having the jumper selected for battery backup when using anything other than low-power-standby SRAMs (such as EPROMs, or PEROMs) will result in the rapid draining of the on-board battery.

Silicon Disk Address Selection

The base address for the silicon disk can be selected by jumpering **J34** pins 11-18, as shown in the following chart.

J34 Base Address Selection Jumper				
Address	17-18	15-16	13-14	11-12
C800	X	X	open	X
CC00	X	X	open	open
D000	X	open	X	X
D400	X	open	X	open
D800	X	open	open	X
DC00	X	open	open	open
E000	open	X	X	X

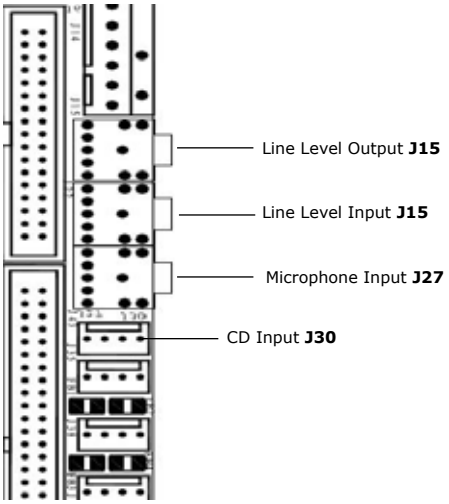
Audio Interface

Visual Index

The EBC-C3PLUS has an audio interface designed to provide high-quality voice reproduction for embedded systems use. The EBC-C3PLUS provides a line level input, line level output, microphone, and a secondary line level input for CD use.

Line Level Output

Line level outputs are provided through the 3.5 mm miniature stereo phone jack at **J15**. This output is a standard 1V p-p line level signal for output to an amplifier or powered speakers.



Line Level Input

Line level inputs are provided through the 3.5 mm miniature stereo phone jack at **J22**. This input accepts standard 1V p-p line level signals from receivers, tape decks, CD players, etc. This input allows for true stereo recording.

Microphone Input

Microphone input connection is made through the 3.5 mm miniature stereo phone jack at **J27**. A low-cost, low-impedance (600Ω) cassette recorder microphone should give satisfactory performance. Note that the microphone input in monophonic and if stereo recording is required, the line level inputs must be used.

CD Input

A secondary line level input is also provided at **J30**. This input is designed primarily for feeding the CD-ROM audio output to the board for multimedia presentations. The pin definitions for **J30** are:

J30

1 o	CD Left Channel IN
2 o	GND
3 o	GND
4 o	CD Right Channel IN

Remote Speaker

Visual Index

If the on-board speaker is not needed, there is a population option for a remote speaker on the EBC-C3PLUS located at **J51**. Contact WinSystems for details.

Serial Interface

Visual Index

The EBC-C3PLUS provides four 16550 compatible RS-232 serial ports, COM1 through COM4.

COM3 and COM4 are RS-232 only and can be enabled or disabled via the jumper block at **J39** pins 1-4. The jumpering for COM3 and COM4 and the addresses they use are shown in the following chart.

J39	J39	COM3 Address	COM4 Address
open	open	Disabled	Disabled
1-2	3-4	3E8H	2E8H
open	3-4	3A8H	2E8H
1-2	open	3A8H	2A8H

COM3 and COM4 Configuration - RS-232 - COM3 and COM4 are RS-232 only and are terminated at **J40**. An adapter cable is available from WinSystems, part number CBL-173-1, which adapts **J40** to two standard DB9M connectors. The pin definitions for **J40** are:

J40

COM3 DCD	**1 o o 2**	COM3 DSR
COM3 RX	**3 o o 4**	COM3 RTS
COM3 TX	**5 o o 6**	COM3 CTS
COM3 DTR	**7 o o 8**	COM3 RI
GND	**9 o o 10**	N/C
COM4 DCD	**11 o o 12**	COM4 DSR
COM4 RX	**13 o o 14**	COM4 RTS
COM4 TX	**15 o o 16**	COM4 CTS
COM4 DTR	**17 o o 18**	COM4 RI
GND	**19 o o 20**	N/C

COM1 and COM2 Configuration - Both COM1 and COM2 can be individually configured for any one of the following operating modes in the BIOS.

1. RS-232 Mode
2. RS-422 Mode with RTS transmitter enable
3. RS-422 Mode with auto transmitter enable
4. RS-485 Mode with RTS transmitter enable
5. RS-485 Mode with RTS transmitter enable and echo back
6. RS-485 Mode with auto transmitter enable
7. RS-485 Mode with auto transmitter enable and echo back

Modes 2, 4 and 5 require the RTS bit (MCR Bit 1) be set in order to transmit. Mode 4 requires that RTS (MCR Bit 1) be de-asserted in order to receive.

Each of the RS-422/RS-485 modes also allows for jumper selection of transmit and/or receive termination resistor(s). There is a 6-pin configuration jumper for COM1 and COM2 that allows the user to select the operating mode and its optional features and termination. The jumper numbers and corresponding port numbers are shown on the following pages. There are three choices for termination when RS-422 or RS-485 modes are used.

TX(100): Places a 100Ω resister across the TX+/TX- pair
RX(100): Places a 100Ω resistor across the RX+/RX- pair
TX/RX(300): Places a 100Ω Resistor from +5V to TX/RX+, a 100Ω resistor from TX/RX- to ground and a 100Ω resistor between TX/RX+and TX/RX-.

COM1 RS-232/RS-422/RS-485 Mode Selection - COM1 is configured using its specific jumper block. The table below shows the appropriate jumpering for the various modes.

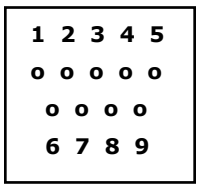
Mode #	Description	J18	J21	Termination		
				J26	J23	J26
				TX(100)	RX(100)	TX/RX (300)
1	RS-232	1-2	Open	N/A	N/A	N/A
2	RS-422 RTS Enable	3-4	5-6	3-4	1-2	1-2 3-4 5-6
3	RS-422 Auto Enable	5-6 (one node must use TX/RX 300 Termination	5-6	N/A	1-2	1-2 3-4 5-6
4	RS-485 RTS Enable	3-4	1-2	3-4	N/A	1-2 3-4 5-6
5	RS-485 RTS Enable with Echo-Back	3-4	3-4	3-4	N/A	1-2 3-4 5-6
6	RS-485 Auto Enable	5-6 (one node must use TX/RX 300 Termination	1-2	3-4	N/A	1-2 3-4 5-6
7	RS-485 Auto Enable with Echo-Back	5-6 (one node must use TX/RX 300 Termination	3-4	N/A	N/A	1-2 3-4 5-6

COM2 RS-232/RS-422/RS-485 Mode Selection - COM2 is configured using its specific jumper block. The table below shows the appropriate jumpering for the various modes.

Mode #	Description	J17	J20	Termination		
				J25	J28	J26
				TX(100)	RX(100)	TX/RX (300)
1	RS-232	1-2	Open	N/A	N/A	N/A
2	RS-422 RTS Enable	3-4	5-6	3-4	1-2	1-2 3-4 5-6
3	RS-422 Auto Enable	5-6 (one node must use TX/RX 300 Termination	5-6	N/A	1-2	1-2 3-4 5-6
4	RS-485 RTS Enable	3-4	1-2	3-4	N/A	1-2 3-4 5-6
5	RS-485 RTS Enable with Echo-Back	3-4	3-4	3-4	N/A	1-2 3-4 5-6
6	RS-485 Auto Enable	5-6 (one node must use TX/RX 300 Termination	1-2	3-4	N/A	1-2 3-4 5-6
7	RS-485 Auto Enable with Echo-Back	5-6 (one node must use TX/RX 300 Termination	3-4	N/A	N/A	1-2 3-4 5-6

Serial I/O Port Definitions - The EBC-C3PLUS terminates its serial ports through the multi-I/O connector at **J43**. WinSystems has available a breakout cable, CBL-247-1, that connects from the 50-pin multi-I/O connector to two 9-pin D-Sub male connectors. When using the standard WinSystems cable, the 9-pin D-Sub pin definitions for each of the three major operation modes are:

DB9 Male



RS-232 Modes	RS-422 Modes	RS-485 Modes
1. DCD	1. N/A	1. N/A
2. RX	2. TX+	2. TX/RX+
3. TX	3. TX-	3. TX/RX-
4. DTR	4. N/A	4. N/A
5. GND	5. GND	5. GND
6. DSR	6. RX+	6. N/A
7. RTS	7. RX-	7. N/A
8. CTS	8. N/A	8. N/A
9. RI	9. N/A	9. N/A

BIOS Supplemental

General Information

The EBC-C3PLUS comes equipped with a standard Award BIOS with setup in ROM that allows users to modify the basic system configuration. This type of information is stored in battery backed CMOS RAM, which allows retention of setup information when power is turned off.

Entering Setup

To enter setup, power up the computer and press the **DEL** key immediately after the message **Press DEL for Setup** appears on the lower left of the screen. If the message disappears before you respond and you still wish to enter setup, restart the system by turning it OFF and then ON or by pressing the **RESET** button, if so equipped, or by pressing the **CTRL, ALT and DEL** keys simultaneously. Alternately, under certain error conditions of incorrect setup, the message:

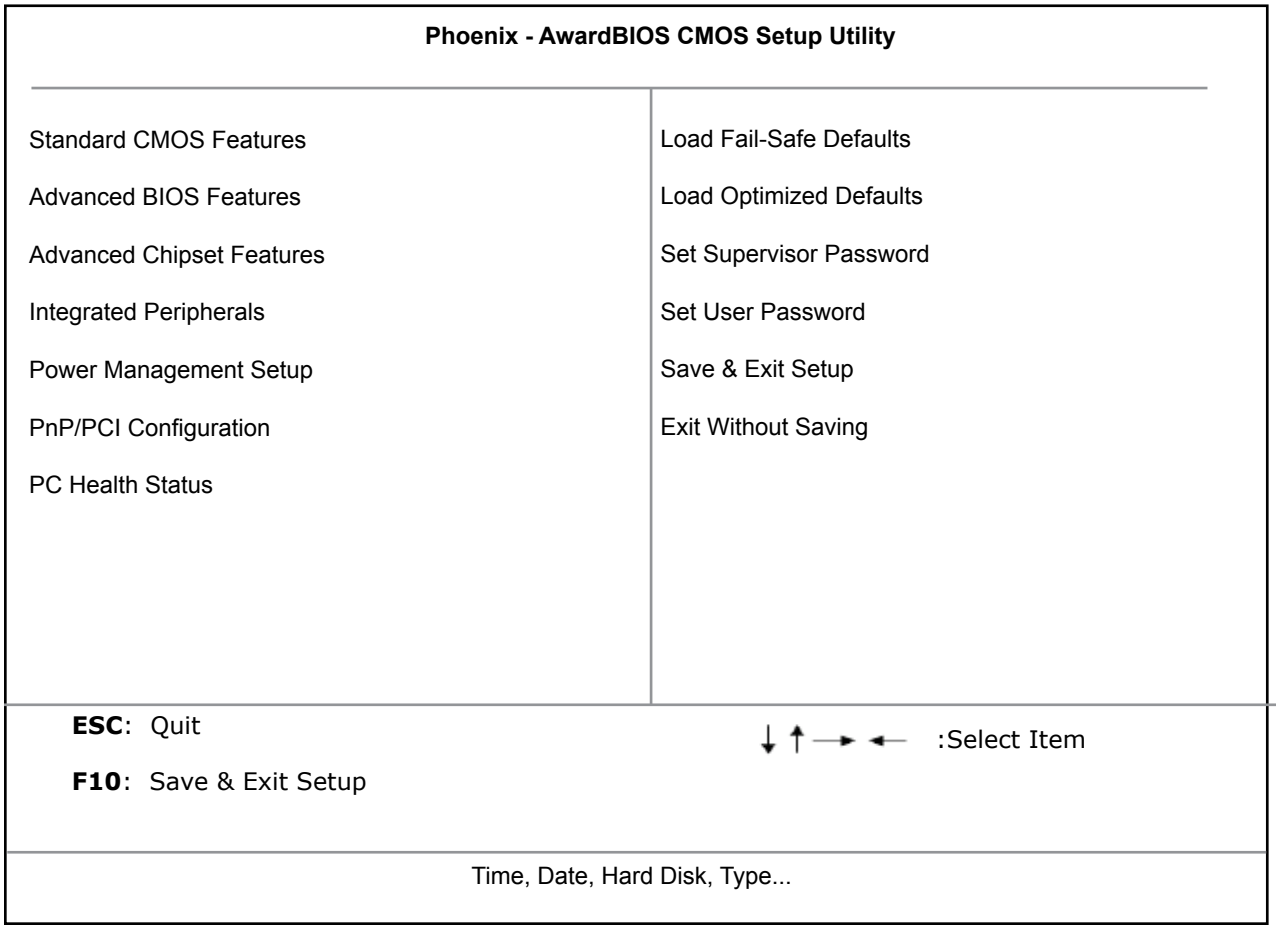
Press F1 to continue or DEL to Enter Setup

may appear. To enter setup at that time, press the **DEL** key. To attempt to continue ignoring the error condition, press the **F1** key.

Setup Main Menu

The main menu screen is displayed below. Each of the options will be discussed in this section.

Use the arrow keys to highlight the desired selection and press **ENTER** to enter the sub-menu or to execute the function selected.



Standard CMOS Features

The items in the Standard CMOS Setup menu are divided into several categories. Each category may include one or many setup items. Use the arrow keys to highlight the item and then use the **PgUp**, **PgDn**, **+**, **-** keys to select the desired value for the item.

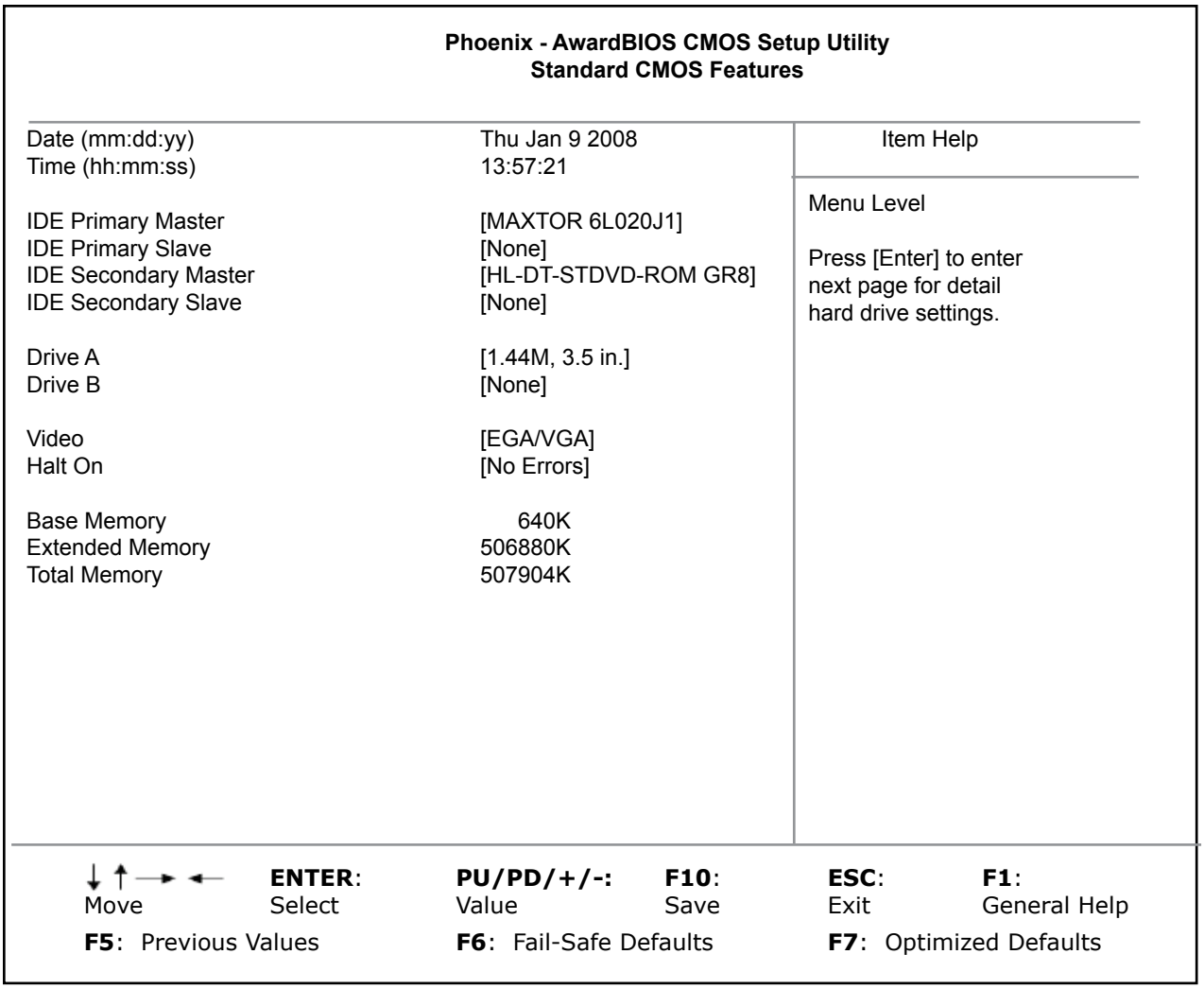
Date

The date format is <*day*>, <*date*>, <*month*>, <*year*>

- *Day* = The day, from Sun to Sat, determined by the BIOS and is display only
- *Date* = The date, from 1 to 31 (or the maximum for the current month)
- *Month* = The month, Jan through Dec
- *Year* = The year from 1900 to 2099

Time

The time is *hour:minute:second*. The time is calculated on the 24-hour, military-time clock such that 1:00 PM is 13:00:00.



IDE Primary Master Pressing **ENTER** brings up a sub-menu screen of choices regarding the Primary fixed disk.

IDE HDD Auto-Detection — Pressing **ENTER** when this selection is highlighted will cause the system to interrogate the attached hard disk and choose the parameters automatically.

IDE Primary Master — Pressing **ENTER** when this item is highlighted allows for selection of how parameters for the hard drive will be determined. The choices are:

- *None* - No Hard Drive is installed
- *Auto* - Automatically detect the hard disk parameters at power up. (recommended setting)
- *Manual* - Use the parameters entered manually by the user.

Access Mode — Pressing **ENTER** when this option is highlighted allows selection of the hard disk access mode. The choices are:

- *CHS* - The drive will be accessed using direct Cylinder, Head, Sector mode. No translation will take place. This can only be used when the "manual" mode is selected above.
- *LBA* - This selection allows the native mode of the drive to be translated to Cylinder, Head and Sector counts that are compatible with allowable BIOS parameter restrictions. Drives up to 120 GB can be used with this mode.
- *LARGE* – This is another translation scheme that is not commonly used but may be required for some O/Ss.
- *AUTO* - This mode chooses the appropriate translation mode (usually LBA) for the actual drive attached. (recommended setting)

Drive Parameters/Size — The drive size in MB is displayed for all modes. When manual and CHS modes are selected, the user may enter values in these fields:

Cylinder	- 0 to 65535
Head	- 0 to 255
Precomp	- 0 to 65535
Landing Zone	- 0 to 65535
Sector	- 0 to 255

IDE Primary Slave This selection is identical to the IDE Primary Master shown above.

IDE Secondary Master This selection is identical to the IDE Primary Master shown above.

IDE Secondary Slave This selection is identical to the IDE Primary Master shown above.

Drive A type/ Drive B type

This category identifies the type of floppy drives attached at Drive A: or Drive B:. The choices are:

NONE
360K, 5.25"
1.2M, 5.25"
720K, 3.5"
1.44M, 3.5"
2.88M, 3.5"

Video

This category specifies the type of video adapter used for the primary system monitor that matched your video display board and monitor. The available choices are:

EGA/VGA
CGA40
CGA80
MONO

The EBC-C3PLUS has built-in VGA support to EGA/VGA should be selected.

Error Halt

This category determines whether the system will halt if a nonfatal error is detected during the power-up self test. The choices are:

- *No Errors* - The systems will not be stopped for any error that may be detected.
- *All Errors* - Whenever the BIOS detects a nonfatal error, the system will be stopped and a prompt will appear.
- *All, but Keyboard*- The system will not stop for a keyboard error, it will stop for all other errors.
- *All, but Diskette* - The systems will not stop for disk errors. All others will result in a prompt.
- *All, but Disk/Key* - All errors except diskette or keyboard will result in a halt and a prompt.

Memory

This category is display only and is determined by the BIOS POST (Power-On Self Test).

Base Memory

The POST routines in the BIOS will determine the amount of base (conventional) memory installed in the system. The value of the base memory is typically 640 KB for systems with a megabyte of memory or greater.

Extended Memory

The BIOS determines how much extended memory is present during the POST. This is the amount of memory located above 1 MB in the CPU's memory address space.

Total Memory

The BIOS displays the total of the Base memory and the Extended memory installed in the system.

Advanced BIOS Features Setup

Phoenix - AwardBIOS CMOS Setup Utility
Advanced BIOS Features

Virus Warning	[Disabled]	Item Help
CPU Internal Cache	[Enabled]	
External Cache	[Enabled]	Menu Level
Quick Power On Self Test	[Enabled]	
First Boot Device	[Floppy]	Allows you to choose the VIRUS warning feature for IDE hard disk boot sector preparation. If this function is enabled and someone attempts to write data into this area, BIOS will show a warning message on screen and alarm beep.
Second Boot Device	[HDD-0]	
Third Boot Device	[CD-ROM]	
Boot Other Device	[Enabled]	
Swap Floppy Drives	[Disabled]	
Boot Up Floppy Seek	[Disabled]	
Boot Up Numlock Status	[On]	
Gate A20 Options	[Fast]	
Typematic Rate Setting	[Enabled]	
Typematic Rate (Chars/Sec)	[6]	
Typematic Delay (Msec)	[250]	
Security Option	[Setup]	
OS Select for DRAM > 64 MB	[Non-OS2]	
Video BIOS Shadow	[Enabled]	
C8000-CBFFF Shadow	[Disabled]	
CC000-CFFFF Shadow	[Disabled]	
D0000-D3FFF Shadow	[Disabled]	
D4000-D7FFF Shadow	[Disabled]	
D8000-DBFFF Shadow	[Disabled]	
DC000-DBFFF Shadow	[Disabled]	
Small Logo (EPA) Show	[Disabled]	

↓ ↑ → ←: Move **ENTER**: Select **PU/PD/+/-:** Value **F10**: Save **ESC**: Exit **F1**: General Help

F5: Previous Values **F6**: Fail-Safe Defaults **F7**: Optimized Defaults

Virus Warning This option, when enabled, protects the boot sector and partition table of the bard disk against unauthorized writes through the BIOS. Any attempt to alter these areas will result in an error message and a prompt to authorize the activity.

CPU Internal Cache This option, when enabled, provides maximum performance by caching instructions and data using the on-chip cache of the Pentium processor.

External Cache This option, when enabled, further enhances performance by caching recently used instructions and data into fast SRAM.

Quick Power on Self Test(POST) This option, when enabled, speeds up the POST during power up. The BIOS will shorten and/or skip some items during POST.

First Boot Device

This option allows for selection of the primary of "First" boot device. The BIOS will attempt to boot from this device first. The menu selections are:

Floppy	*HDD-1*
LS120	*HDD-2*
HDD-0	*HDD-3*
SCSCI	*ZIP100*
CD-ROM	*LAN*
	DISABLED

NOTE: Not all of these devices will be available and selection of a nonexistent device may result in a drastic increase in boot time.

Second Boot Device

This option allows for selection of the secondary choice for boot media usage. The options are identical to those given above for the First Boot Device.

Third Boot Device

This option allows for selection of a third choice of boot media. The options are the same as for the previous two menu items.

Boot Other Device

This option when enabled allows other devices with self-contained boot firmware to become the primary boot media.

Swap Floppy Drive

This option allows for swapping of the A: and B: floppy drive without actually relocating the drives on the cable.

Boot Up Floppy Drive

During POST, when this option is enabled, the BIOS will determine if the floppy drive is 40 tracks or 80 tracks. If disabled, no seek test will be performed and no error can be reported.

Boot Up Numlock Status

This allows user selection of the Numlock state at boot time.

Gate A20 Option

This option allows for the selection of the source for the gate A20 signal. The choices are:

- *Normal*- Sourced from the keyboard controller
- *Fast* - Sourced from the Chipset

Typematic Rate Setting

This option enables or disables the typematic rate programming at boot time. Typematic is the auto-repeat function for the keyboard.

Typematic Rate

When the typematic rate setting in enabled, the typematic repeat speed is set via this option. The supported rates are:

6 characters per second	*15 characters per second*
8 characters per second	*20 characters per second*
10 characters per second	*24 characters per second*
12 characters per second	*30 characters per second*

Typematic Delay

When typematic rate setting is enabled, the option specifies the time in milliseconds before auto-repeat begins. The supported values are:

250 mS *750 mS*
500 mS *1000 mS*

NOTE: Not all of these devices will be available and selection of a nonexistent device may result in a drastic increase in boot time.

Security Option

This option allows you to limit access to the system and setup, or just to setup. The choices are:

- *System*- The system will not boot and access will be denied if the correct password is not entered at the prompt.
- *Setup* - They system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

NOTE: To disable security, select "Password Setting" at the Setup Main Menu and then you will be asked to enter a password. Do not type anything, just hit ENTER. Once the security is disabled, the system will boot and you can enter setup freely.

OS Selection for DRAM>64 MB

This option allows selection of an operating system for DRAM greater then 64 MB. The options are:

OS2
Non-OS2

Shadowing Options

When shadowing for a particular address range is enabled, it instructs the BIOS to copy the BIOS located in ROM into DRAM. This shadowing from an 8-bit EPROM into fast 32-bit DRAM results in a multi-magnitude increase in performance. The main BIOS is shadowed automatically but there are other areas that may be selected for shadowing as shown here:

Video BIOS Shadow – C000-C7FFF EGA/VGA BIOS ROM
C8000-CBFFF
CC000-CFFFF
D0000-D3FFF
D4000-D7FFF
D8000-DBFFF
DC000-DFFFF

Small Logo (EPA) Show

This option, when enabled, instructs the BIOS to display the EPA Energy Star logo in the upper right corner of the screen during the POST process.

Advanced Chipset Features Setup

Phoenix - AwardBIOS CMOS Setup Utility
Advanced Chipset Features

DRAM Timing By SPD	[Enabled]	Item Help
DRAM Clock	[Host CLK]	
SDRAM Cycle Length	[3]	Menu Level
Bank Interleave	[Disabled]	
Memory Hole	[Disabled]	
P2C/C2P Concurrency	[Enabled]	
System BIOS Cacheable	[Disabled]	
Video RAM Cacheable	[Disabled]	
Frame Buffer Size	[16M]	
AGP Aperture Size	[64M]	
AGP-4X Mode	[Enabled]	
AGP Driving Control	[Manual]	
AGP Driving Value	[DA]	
Select Display Device	[CRT]	
TV Type	[US NTSC]	
Panel Type	[07]	
Onchip USB	[Enabled]	
USB Keyboard Support	[Disabled]	
OnChip Sound	[Auto]	
CPU to PCI Write Buffer	[Enabled]	
PCI Dynamic Bursting	[Enabled]	
PCI Master 0 WS Write	[Enabled]	
PCI Delay Transaction	[Disabled]	
PCI #2 Access #1 Retry	[Enabled]	
AGP Master 1 WS Write	[Disabled]	
AGP Master 1 WS Read	[Disabled]	

↓ ↑ → ← Move **ENTER**: Select **PU/PD/+/-:** Value **F10**: Save **ESC**: Exit **F1**: General Help

F5: Previous Values **F6**: Fail-Safe Defaults **F7**: Optimized Defaults

The options in this section control the chipset programming at boot time. In most cases, the default settings should be used unless you have a clear understanding of the significance of the change. It is possible using these options to create a system that will either not boot or is very unstable or unreliable. If this should occur, there are two methods to return the system to a stable configuration. If the system works well enough to get into setup, simply choose the **Load BIOS Defaults** option and then select **Save and Exit setup** to restore factory defaults. If the system will not run well enough to run setup, it will be necessary to remove the battery source temporarily until the CMOS memory decays. Refer to Real Time Clock/Calendar section for details on reinitializing the CMOS RAM.

Each of the options for the Advanced Chipset Features Menu will be briefly discussed in the sections that follow.

DRAM Timing by SPD This option, when enabled, allows for selection of DRAM timing with modules that support a serial port device. When using a DRAM module without serial port support, the following parameters must be set to match the users memory device.

DRAM Clock This option controls the DRAM Clock. When DRAM timing by SPD is disabled, the following options are available:

Host Clock
HCLK-33M

SDRAM Cycle Length This option allows for setting the SDRAM Cycle length timing. The choices are:

3 clocks
2 clocks

Bank Interleave This option allows for setting of the Bank Interleave. Since WinSystems' boards only support one bank of memory, this option should be left disabled. The choices are:

Disabled
2 Bank
4 Bank

Memory Hole This option, when enabled, disabled on-board memory between 15 MB and 16 MB.

P2C/C2P Concurrency This option allows for selection of the P2C/C2P concurrency. The options are:

Enabled
Disabled

System BIOS Cacheable This option enables or disables cacheability of the system BIOS.

Video RAM Cacheable This option allows for cacheability of the video RAM.

Frame Buffer Size This option allows for selection of the frame buffer size. The choices are:

N/A	*8M*
2M	*16M*
4M	*32M*

AGP Aperture Size (MB) This option specifies the amount of address space to allocate to the AGP video aperture. The choices are:

4	*32*
8	*64*
16	*128*

AGP 4X Mode This option, enables the AGP 4X mode.

AGP Driving Control This option selects the AGP driving control. The choices are:

Auto
Manual

AGP Driving Value This option allows the user to select (enter a hex code) for the AGP driving value when AGP driving control is set to manual.

Select Display Device This option allows selection of the type of display device used. The choices are:

Auto	*TV*
CRT	*CRT + TV*
LCD	*DVI*
CRT + LCD	*CRT + DVI*

TV Type This options allows the selection of the type of TV device used. The choices are:

JP NTSC
US NTSC
PAL

Panel Type This option allows entering of the specific panel type. The choices are:

0 selects	*640 x 480 TFT*
1 selects	*800 x 600 TFT*
2 selects	*1024 x 768 TFT 2 pixel/clk at 32MHz*
3 selects	*1280 x 1024 TFT*
4 selects	*640 x 480 DSTN*
5 selects	*800 x 600 DSTN*
6 selects	*1024 x 768 DSTN*
7 selects	*1024 x 768 TFT*
8 selects	*640 x 480 TFT*
9 selects	*800 x 600 TFT*
A selects	*1024 x 768 TFT*
B selects	*1280 x 1024 TFT*
C selects	*1400 x 1050 TFT 2 pixel/clk at 54MHz*
D selects	*800 x 600 DSTN*
E selects	*1024 x 768 DSTN*
F selects	*1280 x 1024 DSTN*

OnChip USB This option enables or disables the on-chip USB.

USB Keyboard Support This option enables the USB keyboard support.

OnChip Sound This option allows for selection of the on-chip sound feature. The choices are:

Auto
Disable

CPU to PCI Write Buffer This option enables the CPU to PCI write buffer.

PCI Dynamics Bursting This option enables the PCI dynamics bursting.

PCI Maser 0 WS Write This option enables the PCI master 0 wait state write.

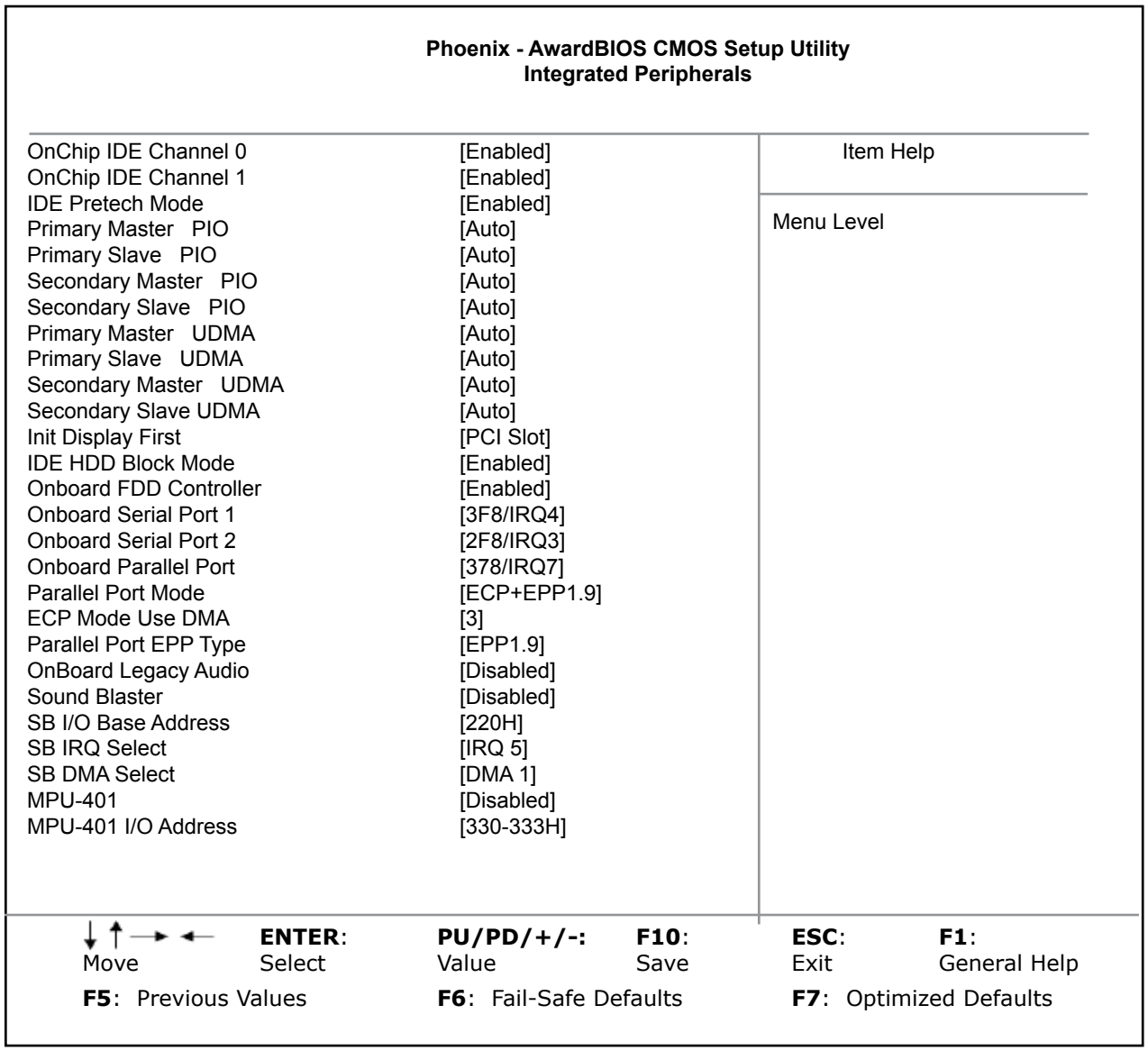
PCI Delay Transaction This option enables the PCI delay transaction.

PCI #2 Access PCI #1 Retry This option enables the PCI#2 access and PCI#1 retry.

AGP Master 1 WS Write This option enables the AGP master 1 wait state write.

AGP Master 1 WS Read This option enables the AGP master 1 wait state read.

Integrated Peripherals



The options in this section allow for control of the integrated peripherals, i.e., floppy and IDE controllers, serial ports, and the parallel port.

OnChip IDE Channel 0 This option enables the OnChip IDE Channel 0.

OnChip IDE Channel 1 This option enables the OnChip IDE Channel 1.

IDE Prefetch Mode This option enables or disables the IDE Prefetch Mode.

Primary Master PIO This option allows selection of the PIO mode to be used with the Primary Master IDE device. The choices are:

Auto	*Mode 3*
Mode 1	*Mode 4*
Mode 2	

Primary Slave PIO This option allows selection of the PIO mode to be used with the Primary Slave IDE device. The choices are:

Auto	*Mode 3*
Mode 1	*Mode 4*
Mode 2	

Secondary Master PIO This option allows selection of the PIO mode to be used with the Secondary Master IDE device. The choices are:

Auto
Mode 1
Mode 2
Mode 3
Mode 4

Secondary Slave PIO This option allows selection of the PIO mode to be used with the Secondary Slave IDE device. The choices are:

Auto
Mode 1
Mode 2
Mode 3
Mode 4

Primary Master UDMA This option selects whether an UDMA mode will be used for disk transfers on the Primary Master IDE device. The choices are:

Disabled
Auto

Primary Slave UDMA This option selects whether an UDMA mode will be used for disk transfers on the Primary Slave IDE device. The choices are:

Disabled
Auto

Secondary Master UDMA This option selects whether an UDMA mode will be used for disk transfers on the Secondary Master IDE device. The choices are:

Disabled
Auto

Secondary Slave UDMA This option selects whether an UDMA mode will be used for disk transfers on the Secondary Slave IDE device. The choices are:

Disabled
Auto

Init Display First This option allows selection of the source for the first, or primary, video controller. The choices are:

PCI Slot
AGP

NOTE: The on-board video is implemented on the AGP bus. An alternate primary video display may be used by installing a PC/104-*Plus* video card and setting this option to PCI slot.

IDE Block Mode This option allows enabling of the IDE block mode for disk transfers.

Onboard FDC Controller This option controls the onboard Floppy Disk controller. The options are:

Enabled
Disabled

Onboard Serial Port 1 This option controls of the first on-board serial port. The options are:

Disabled
3F8/IRQ4
2F8/IRQ3
3E8/IRQ4
2E8/IRQ3
Auto

Onboard Serial Port 2 This option controls the second on-board serial port. The options are:

Disabled
3F8/IRQ4
2F8/IRQ3
3E8/IRQ4
2E8/IRQ3
Auto

Onboard Parallel Port This option allows for configuration of the on-board parallel printer port. The options are:

Disabled
3BC/IRQ7
378/IRQ7
278/IRQ5

Onboard Parallel Port This option controls the operating mode of the on-board parallel port. The options are:

Normal
EPP
ECP
ECP/EPP

ECP Mode Use DMA This option controls which DMA channel will be used for ECP transfers. The choices are:

3
1

Parallel Port EPP Type This option selects the Parallel Port EPP type. The choices are:

EPP1.9
EPP1.7

Onboard Legacy Audio This option enables the Onboard Legacy Audio. The choices are:

Disabled
Enabled

Sound Blaster This option enables the onboard Sound Blaster. The choices are:

Disabled
Enabled

SB I/O Base Address This option selects the Sound Blaster Base I/O address. The choices are:

220H
240H
260H
280H

SB IRQ Select This option selects the Sound Blaster interrupt request. The choices are:

IRQ5
IRQ7
IRQ9
IRQ10

SB DMA Select This option selects the Sound Blaster DMA channel. The choices are:

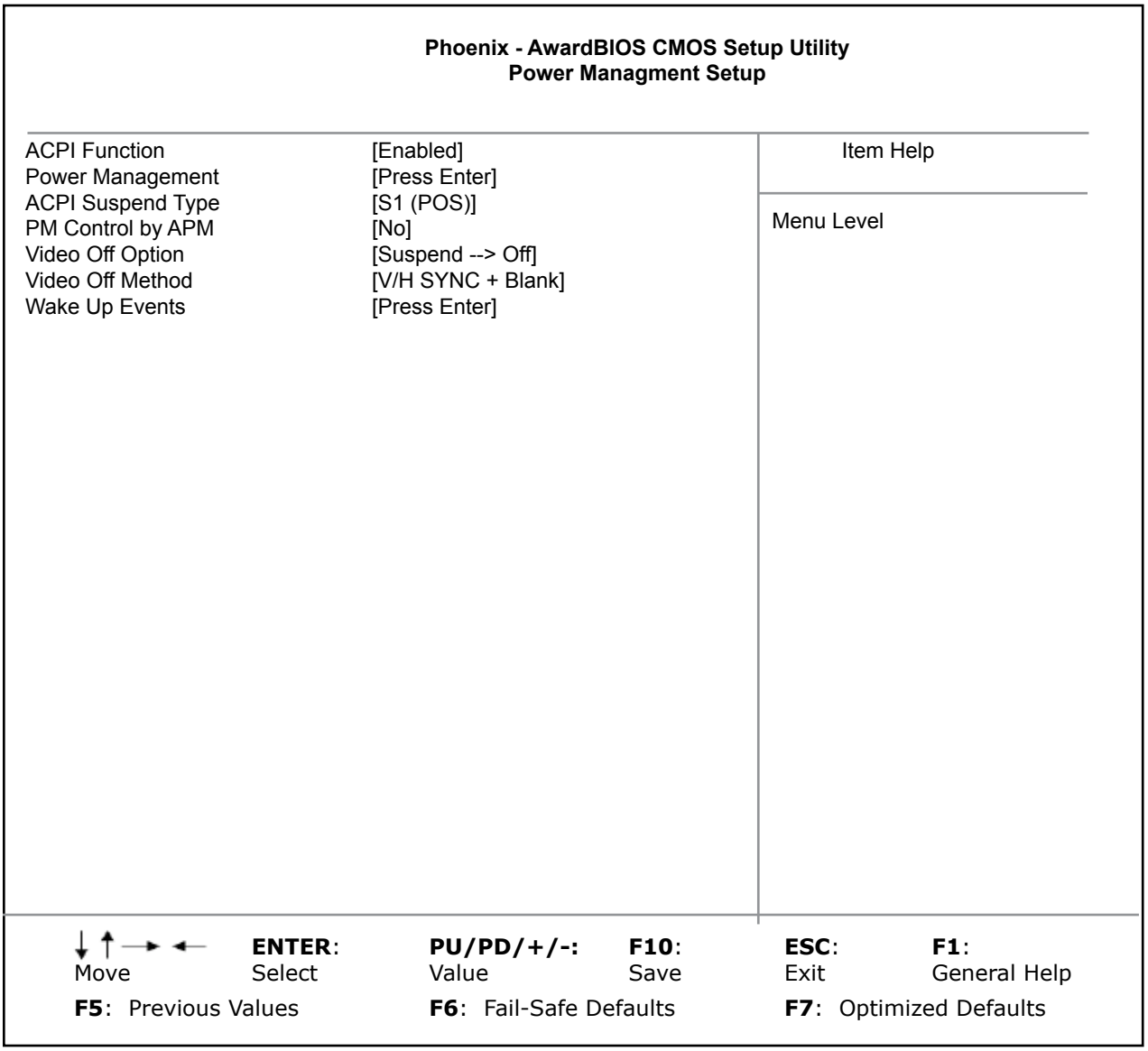
DMA0
DMA1
DMA2
DMA3

MPU-401 This option enables the MPU-401.

MPU-401 I/O Address This option selects the MPU-401 I/O address. The choices are:

300-303H
310-313H
320-323H
330-333H

Power Management Setup



The items in this menu control operation of the BIOS based power management functions.

ACPI Function This option controls the BIOS level ACPI functionality.

Power Management This option specifies the type and extent of power management options. The choices are:

User Define
Min Saving
Max Saving

ACPI Suspend Type This option allows for selection of the ACPI suspend type. The choices are:

S1 (POS)
S3 (STR)

PC Control by APM

This option, when enabled, allows an APM-aware OS to control system power management. The options are:

Yes
No

Video Off Option

This option specifies at what power-management stage the video off function will be executed. The options are:

Always On
Suspend -> Off
All Modes -> Off

Video Off Method

This option specifies the method used for Video blanking or PM shutdown. The options are:

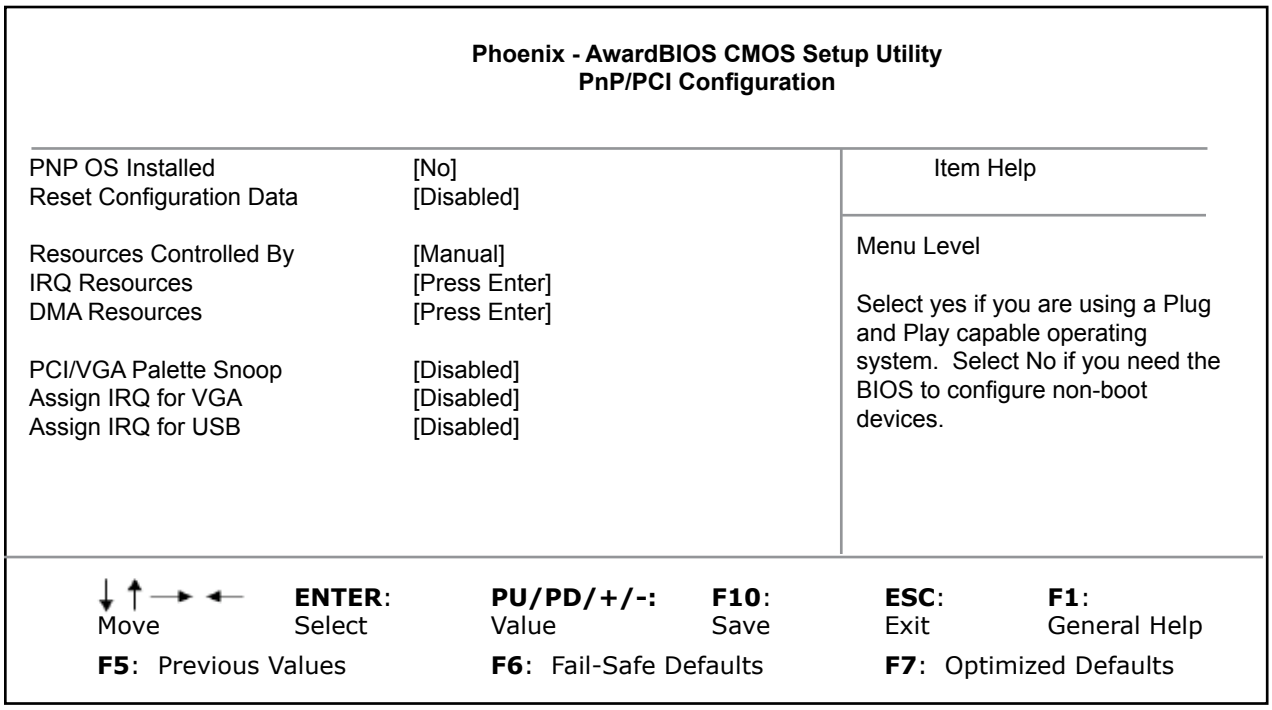
Blank Screen
V/H SYNC + Blank
DPMS Support

Wake Up Events

The eight options that follow allow individual selection of IRQs or devices to monitor. Activity on any of the enabled options resets the countdown timers delaying any further power management steps. The items that can be enabled for monitoring are:

VGA
LPT & COM
HDD & FDD
PCI Master
Modern Ring Resume
RTC Alarm Resume
Primary INTR
IRQs Activity Monitor

PnP/PCI Configurations



PnP OS Installed This option allows the used to assign whether the operation system is Plug-and-Play compatible. The choices are:

Yes
No

Reset Configuration Data This option, when enabled, will reset the configuration data on power up. The choices are:

Enabled
Disabled

Resources Controlled By This option allows the user to select resource control of the system. The choices are:

Auto (ESCD)
Manual

IRQ Resources This option allows for IRQs to be reserved for legacy ISA devices or to be used in the pool of available IRQs for PCU and ISA PnP devices.

DMA Resources This option allows for DMA resources to be reserved for legacy ISA devices or to be used in the pool of available DMA resources for PCU or ISA PnP devices.

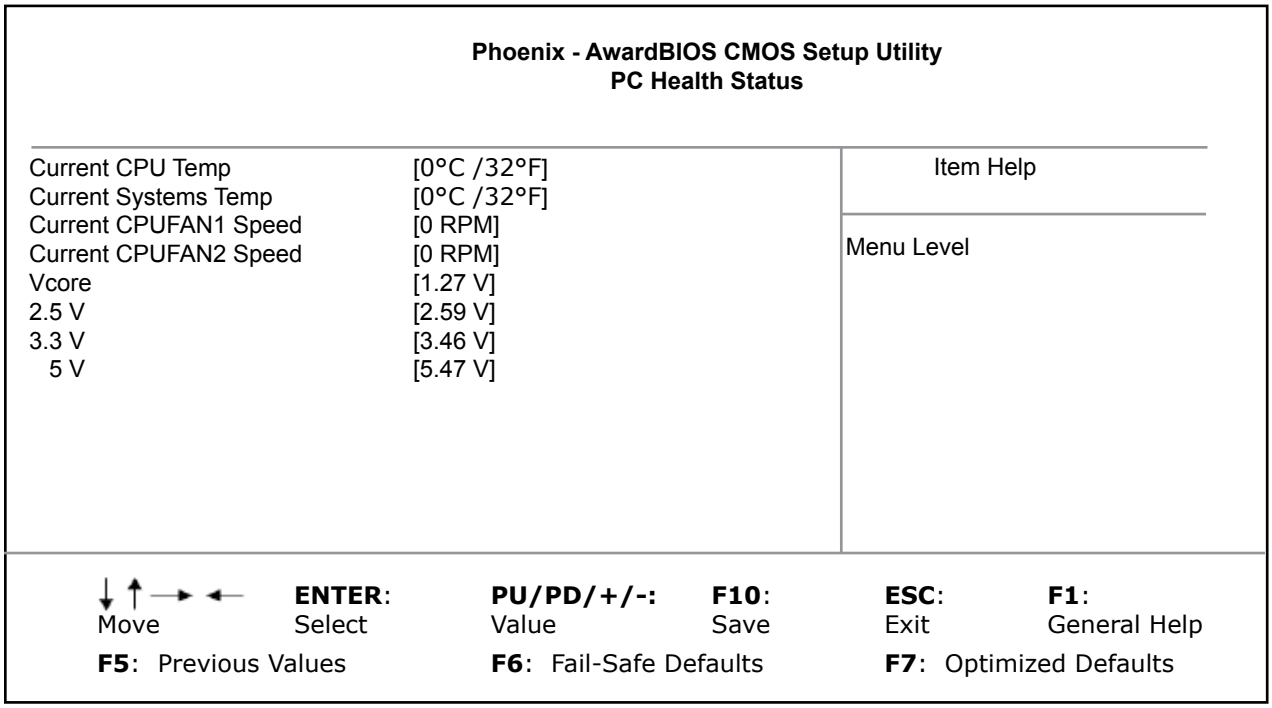
PCI/VGA Palette Snoop This option, when enabled, permits PCI/VGA palette snooping.

Assign IRQ for VGA This option enables the Interrupt Request for VGA.

Assign IRQ for USB This option enables the Interrupt Request for USB.

PC Health Status

This option is different from the other setup menu items in that there are no configurable options. This is simply a status screen that can be used to examine the status of various temperatures and voltages on the board.



Load Fail-Safe Defaults

This option, when selected, reloads all of the CMOS settings with the fail-safe default settings.

Load Optimized Defaults

This option, when selected, reloads all of the CMOS setting with the optimized default settings.

Set Supervisor Password

This option, when a password has been entered, protects the setup menus from unauthorized alteration of the options. Hitting **ENTER** when prompted for the password, disables the password security.

Set User Password

This option provides a second level of password security to the BIOS setup screens. When both the supervisor and the user passwords are enabled, the user will only be able to alter fixed disk information. If no supervisor password is enabled, the user access password allows full access to the setup screens. The security option is disabled by hitting **ENTER** at the password prompt.

Save & Exit Setup

This function writes all changes to CMOS RAM and restarts the system.

Exit Without Saving

This option exits setup without saving any changes made and the restarts the system.

Silicon Disk Reference

DiskOnChip® Usage

The EBC-C3PLUS supports the SanDisk DiskOnChip® (DOC) flash device in various sizes. The DOC device contains a BIOS extension, the TFFS (True Flash File System), and the Flash memory all in a single 32-pin device. The DOC emulates a hard disk and can be used as a secondary hard disk to a physical IDE drive or it can be the only hard disk in the system.

The DOC is installed in the socket at **U28**. Refer to the Silicon Disk Configuration Section for correct device jumpering and enabling of the DOC.

DiskOnChip® Initialization

The DOC is initialized in an identical fashion to a fixed disk. DOS is booted (from floppy or hard disk), FDISK is run on the DOC drive (be sure to confirm the correct drive), the system is rebooted and then the DOC is formatted using the DOS format command.

If the /S switch was used during formatting and there is not another fixed disk device specified or attached to the system, the DOC will become the boot device. If a hard disk is present, the DOC will become a secondary fixed disk.

Nonbootable RAMDISK Usage

A nonbootable RAMDISK can be used for program updates, parameter storage, or data logging applications. A nonbootable RAMDISK uses the WinSystems Universal Solid State Disk Driver (USSD) which is loaded via the boot media's CONFIG.SYS file with the entry:

device = ussd.sys/mod:p /pad:1ec /seg:DC00/psz:16/inc:1/spg:80/dsz:512

The nonbootable RAMDISK is installed into the socket at **U28**. Refer to the Silicon Disk Configuration Section for correct device jumpering and enabling of the RAMDISK.

Nonbootable FLASHDISK Usage

The Atmel 5 volt flash parts (29C040/29C040A) may also be used as a nonbootable drive in a manner nearly identical to the RAMDISK usage described above. The only change when using USSD for the Atmel PEROMs is the addition of the /EPt:256 parameter to the CONFIG.SYS line which installs the USSD driver. An example using a 512 KB EPROM for a ROMDISK and a 512 KB PEROM device would need the line:

device = ussd.sys/mod:p /pad:1ec /seg:DC00/psz:16/inc:1/spg:80/dsz:512/ept:256

in the CONFIG.SYS file on the floppy to be imaged.

The nonbootable FLASHDISK is installed into the socket at **U28**. Refer to the Silicon Disk Configuration Section for correct device jumpering and enabling of the FLASHDISK.

WS16C48 Programming Reference

Introduction

This section provides basic documentation for the included I/O routines. It is intended that the accompanying source code equip the programmer with a basic library of I/O functions for the WS16C48 or can serve as the basis from which application specific code can be derived.

Function Definitions

This section describes each of the functions contained in the driver. Where necessary, short examples will be provided to illustrate usage. Any application making use of any of the driver functions should include the header file UIO48.H, which includes the function prototypes and the needed constant definitions.

Note that all of the functions utilize the concept of *bit_number*. The bit_number is a value from 1 to 48 (1 to 24 for interrupt related functions) that correlates to a specific I/O pin. Bit_number 1 is port 0 bit 0 and continues through to bit_number 48 at port 5 bit 7.

INIT_IO – Initializes I/O, set all ports to input

Syntax

void init_io(unsigned io_address);

Description

This function takes a single argument:

io_address – The I/O address of the WS16C48 chip.

There is no return value. This function initializes all I/O pins for input (sets them high), disables all interrupt settings, and sets the image values.

READ_BIT – Reads an I/O port Pin

Syntax

int read_bit(int bit_number);

Description

This function takes a single argument:

bit_number – a value from 1 to 48 specifying the I/O pin to read from.

This function returns the state of the I/O pin. A **1** is returned if the I/O pin is low and a **0** is returned if the pin is high.

WRITE_BIT – Writes a **1** or **0** to an I/O Pin

Syntax

void write_bit(int bit_number, int value);

Description

This function takes two arguments:

bit_number – a value from 1 to 48 specifying the I/O pin to be acted upon.

value - is ether 1 or 0.

This function allows for writing of a single bit to either a **0** or a **1** as specified by the second argument. There is no return value and other bits in the I/O port are not affected.

SET_BIT – Sets the specified I/O Pin

Syntax

void set_bit(int bit_number);

Description

This function takes a single argument:

bit_number – a value from 1 to 48 specifying the I/O pin to be set.

This function sets the specified I/O port bit. Note that setting a bit results in the I/O pin actually going low. There is no return value and other bits in the same I/O port are unaffected.

CLR_BIT – Clears the specified I/O Pin

Syntax

void clr_bit(int bit_number);

Description

This function takes a single argument:

bit_number – a value from 1 to 48 specifying the I/O pin to clear.

This function clears the specified I/O bit. Note that clearing the I/O bit results in the actual I/O pin going high. This function does not affect any bits other than the one specified.

ENAB_BIT – Enables Edge Interrupt, Select Polarity

Syntax

void enab_bit(int bit_number, int polarity);

Description

This function takes two arguments:

bit_number – a value from 1 to 24, specifying the appropriate bit.

polarity - specifies rising or falling edge polarity detect. The constraints RISING and FALLING are defined UIO48.H.

This function enables the edge detection circuitry for the specified bit at the specified polarity. It does not unmask the interrupt controller, install vectors, or handle interrupts when they occur. There is no return value and only the specified bit is affected.

DISAB_INT – Disables Edge Detect Interrupt Detection

Syntax

void disab_int(int bit_number);

Description

This function takes a single argument:

bit_number – a value from 1 to 24 specifying the appropriate bit.

This function shuts down the edge detection interrupts for the specified bit. There is no return value and no harm is done by calling this function for a bit which did not have edge detection interrupts enabled. There is no effect on any other bits.

CLR_INT – Clears the specified pending interrupt

Syntax

void clr_int(int bit_number);

Description

This function takes a single argument:

bit_number – a value from 1 to 24 specifying the bit number to reset the interrupt.

This function clears a pending interrupt on the specified bit. It does this by disabling and reenabling the interrupt. The net result after the call is that the interrupt is no longer pending and is renamed for the next transition of the same polarity. Calling this function on a bit that has not been enabled for interrupts will result in its interrupt being enabled with an undefined polarity. Calling this function with no interrupt pending will have no adverse effect. Only the specified bit is affected.

GET_INT – Retrieves bit number of pending interrupt

Syntax

void get_int(void);

Description

This function requires no arguments.

This function returns either a **0** for no bit interrupts pending or a value between 1 and 24 representing a bit number that has a pending edge detect interrupt. The function returns with the first interrupt found and begins its search at Port 0 bit 0 proceeding through to Port 2 Bit 7. It is necessary to use either clr_int() or disab_int() to avoid returning the same bit continuously. This function may be used in an application's ISE or can be used in the foreground to poll for bit transitions.

Sample Programs

There are three sample programs in source code form included on the EBC-C3PLUS diskette in the UIO48 directory. These programs are not useful by themselves but are provided to illustrate the usage of the I/O functions provided in UIO48.C.

FLASH.C

This program was compiled with Borland C/C++ version 3.1 on the command line with:
bcc flash.c uio48.c

This program illustrates the most basic usage of the WS16C48. It uses three functions from the driver code. The io_init() function is used to initialize the I/O functions and the set_bit() and clr_bit() functions are used to sequence through all 48 bits turning each on and then off in turn.

POLL.C

This program was compiled with Borland C/C++ version 3.1 on the command line with:
bcc poll.c uio48.c

This program illustrates additional features of thw WS16C48 and the I/O library functions. It programs the first 24 bits for input, arms them for falling edge detection, and then polls using the library routine get_init() to determine if any transitions have taken place.

INT.C

This program was compiled with Borland C/C++ version 3.1 on the command line with:
bcc int.c uio48.c

This program is identical in function to the POLL.C program except that interrupts are active and all updating of the transition counters is completed in the background during the interrupt service routine.

Summary

Links to the source code for all three programs as well as the I/O routines can be found in the Software Drivers & Examples Section of this manual. These I/O routines along with the sample program should provide for a good basis on which to build an application using the features of the WS16C48.

I/O Port Map

Following is a list of PC I/O ports. Addresses marked with a '-' are not used on the EBC-C3PLUS but their use should be carefully evaluated so as not to conflict with other I/O boards. I/O addresses marked with a '+' are used on the EBC-C3PLUS and are unique to the WinSystems design. I/O addresses marked with '**' are generally unused and should be the basis for the first choices in I/O address selection for external I/O boards.

Hex Range	Usage
000-00F	8327 DMA #1
**010-01F	Free
020-021	8259 PIC #1
+022-023	Finali 486 Chipset Registers
**024-03F	Free
040-043	8254 Timer
**044-05F	Free
060-06F	8042 Keyboard Controller
070-071	CMOS RAM/RTC
**072-07F	Free
080-08F	DMA Page Registers
**090-09F	Free
0A0-BF	8259 PIC #2
0C0-0DF	8237 DMA #2
**0E0-0EF	Free
0F0-0F1	Coprocessor Control
**0F2-11F	Free
+120-12F	WS16C48HDIO
**130-1DF	Free
+1E0-1EF	SSD, LED, Watchdog Control
1F0-1FF	Fixed Disk I/O
-200-20F	Joystick Port
-210-21F	PCM SSD I/O Ports
-220-22F	Soundblaster I/O Ports
*230-237	Free
-238-23B	BUS Mouse
**240-277	Free
278-27F	LPT1
**280-2AF	Free
-2B0-2DF	EGA Video
-2E0-2E7	GPIB Interface
2E8-2EF	COM4
**2F0-2F7	Free
2F8-2FF	COM2
-300-31F	Prototype Card
-320-32F	XT Hard Disk
**330-377	Free
-378-37F	Parallel Printer
-380-3AF	SDLC
-3B0-3BB	DMA
-3C0-3CF	EGA
3E8-3EF	COM3
3F0-3F6	Floppy Disk
3F8-3FF	COM1

Interrupt Map

No.	Address	Type	Description
0	0	CPU	Divide by Zero
1	4	CPU	Single Step
			386 Debug Exception
2	8	CPU	NMI
3	0C	CPU	Breakpoint
4	10	CPU	Overflow
5	14	BIOS	Print Screen
		186	Bounds Exception
6	18	186	Invalid Opcode Exception
7	1C	186	Coprocessor unavailable
8	20	HARDWARE	IRQ 0 - 18.2Hz heartbeat
		286	LIDT - Double fault exception
9	24	HARDWARE	IRQ 1 – Keyboard Interrupt
		286	Coprocessor segment
A	28	HARDWARE	IRQ 2 – XT reserved, AT-Slaved Controller
		286	Invalid TSS exception
B	2C	HARDWARE	IRQ 3 - COM2
		286	Segment not present
C	30	HARDWARE	IRQ 4 - COM1
		286	Stack fault exception
D	34	HARDWARE	IRQ 5 – XT Hard Disk, AT Free
		286	Protection Fault
E	38	HARDWARE	IRQ 6 - Floppy Disk Interrupt
		286	Page fault
F	3C	HARDWARE	IRQ 7 - LPT 1
10	40	BIOS	Video BIOS functions
		286	Coprocessor exception
11	44	BIOS	BIOS equipment check
		486	Alignment check exception
12	48	BIOS	BIOS memory size
13	4C	BIOS	BIOS disk function
14	50	BIOS	BIOS serial functions
15	54	BIOS	BIOS casette/protected misc funtions
16	58	BIOS	BIOS keyboard functions
17	5C	BIOS	BIOS printer functions
18	60	BIOS	SROM Basic Entry (IBM)
19	64	BIOS	BIOS Boot function
1A	68	BIOS	BIOS time of day functions
1B	6C	BIOS	BIOS keyboard break vector
1C	70	BIOS	User chained timer tick
1D	74	BIOS	BIOS video initialization
1E	78	BIOS	BIOS floppy disk parameter table
1F	7C	BIOS	BIOS CGA graphics character font
20	80	MS-DOS	Program Terminate
21	84	MS-DOS	DOS function calls
22	88	MS-DOS	Terminate address
23	8C	MS-DOS	Ctrl-Break address
24	90	MS-DOS	Fatal Error vector
25	94	MS-DOS	Absolute disk read

No.	Address	Type	Description
26	98	MS-DOS	Absolute disk write
27	9C	MS-DOS	Terminate address
28	A0	MS-DOS	Idle signal
29	A4	MS-DOS	TTY output
2A	A8	MS-DOS	MS-Net services
2F	BC	MS-DOS	Print Spool
30	C0	MS-DOS	Long jump interface
33	CC	MS-DOS	Mouse functions
3F	FC	MS-DOS	Overlay interrupt
40	100	BIOS	Floppy I/O when fixed disk is present
41	104	BIOS	BIOS Fixed disk 1 parameter table
42	108	BIOS	EGA Chain
43	10C	BIOS	EGA Parameter table pointer
44	110	BIOS	EGA graphics font
46	118	BIOS	BIOS Fixed disk 2 table
4A	128	BIOS	AT Alarm exit address
50	140	BIOS	AT Alarm interrupt
51	144	BIOS	Mouse functions
5A	168	NET	NET functions
5B	16C	NET	boot chain
5C	170	NET	NET BIOS entry
67	19C	MS-DOS	EMS functions
6D	1B4	VGA	VGA service
70	1C0	HARDWARE	IRQ 8 - Real time clock
71	1C4	HARDWARE	IRQ 9 - Redirected IRQ 2
72	1C8	HARDWARE	IRQ 10 - unassigned
73	1CC	HARDWARE	IRQ 11 - unassigned
74	1D0	HARDWARE	IRQ 12 – unassigned
75	1D4	HARDWARE	IRQ 13 - unassigned
76	1D8	HARDWARE	IRQ 14 - IDE fixed disk
77	1DC	HARDWARE	IRQ 15 - unassigned
80	200		
F0	3C0	BASIC	
F1	3C4		
FF	3CF	NOT USED	

Cables

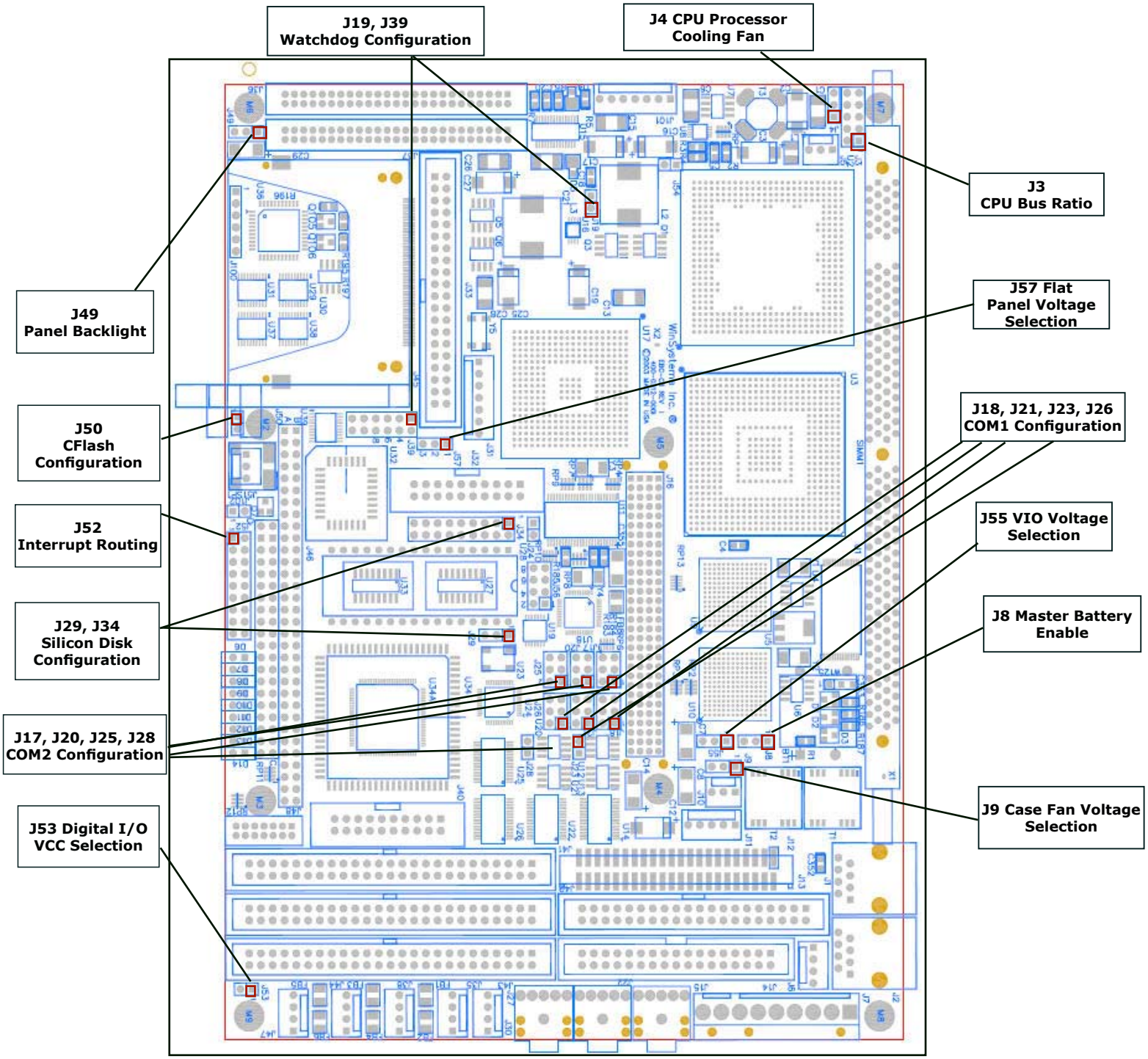
Part Number	Description
CBL-SET-312-1	Various cables for the EBC-C3PLUS includes:
CBL-115-4	4-ft., Opto rack interface
CBL-125-1	Floppy Disk Adapter Cable
CBL-126-10	ATA100 IDE Disk Cable
CBL-173-1	20-pin ribbon to two 9-pin male D connector adapter
CBL-225-1	PS/2 Mouse Adapter
CBL-234-1	14-pin ribbon to 15-pin D-sub CRT adapter
CBL-236-2	Power cable (unterminated)
CBL-247-1	Power cable for SBC (unterminated)
CBL-249-1	4-pin USB Adapter Cable
CBL-266-1	2-mm., 44-pin, IDE 18-in. Cable

Software Drivers & Examples

BIOS Driver	
EBC-C3PLUS BIOS Driver	EBC-C3Plus_BIOS_Driver.zip
CPU Driver	
All-in-one Windows Driver for VIA Chipsets 4.16b	Hyperion4in1v4.zip
All-in-one Windows Driver for VIA Chipsets 4.51	Hyperion4in1v451v.zip
Linux C3 Processor Utilities	C3Processor.zip
Video Driver	
(For Windows)	
Twister Windows XP/2000 version 13.94.12 with Hotkey	139412Hotkey.zip
Twister Windows XP/2000 version 13.94.12 No Hotkey	139412NoHotkey.zip
Twister Windows 9x/ME version 13.00.49 No Install Shield	130049t9NoInstall.zip
Twister Windows 9x/ME version 13.00.49 Install Shield	130049t9Install.zip
Video Driver	
(For Linux)	
Savage Family Linux XFree86 4.0.3 X Server Binary and Switch Utility version 1.1.18	Savage4.0.3_binary.tgz
Savage Family Linux XFree86 4.1.0 X Server Binary and Switch Utility version 1.1.18	Savage4.1.0_binary.tgz
Audio Driver	
Windows and Linux	C3Audio.zip
Ethernet Driver	
(Drivers for 82551ER/82559ER 10/100 Ethernet Controller)	
NDIS 4 (Windows 98)	82559ERWIN98.zip
NDIS 4 (Windows NT4/2000)	e100ndis4.zip
Windows NT Embedded 4.0	e100ent.zip
Windows XP/2000	e100exp.zip
Windows CE 3.0	e100ce3.zip
Windows CE.NET	e100ce.zip
DOS	e100bdos.zip
Linux 2.4, 2.6 10/100 Adapter Base Driver	e100-3.5.14.tar.gz
Linux 2.2, 10/100 Adapter Base Driver	e100-2.1.15.tar.gz
DOS Packet Drivers	packet.zip
Examples	
(For WS16C48 Digital I/O Chip)	
DOS Driver - C Functions	uio48ebc.zip
Linux Drivers - Kernel 2.2, 2.4	linux_uio48_96.zip
Linux Drivers - Kernel 2.6	uio48io_kernel_2.6.zip
Windows XP Driver	wsuio48_96xp.zip
Reprogramming DOS tick for high resolution timing	tickdemo.zip
Serial Console Utilities	
Generic 38400baud Serial console redirect for COM1	scon1.zip
Generic 38400baud Serial console redirect for COM2	scon2.zip
Generic 9600baud Serial console redirect for COM1	sc19600.zip
Generic 9600baud Serial console redirect for COM2	sc29600.zip

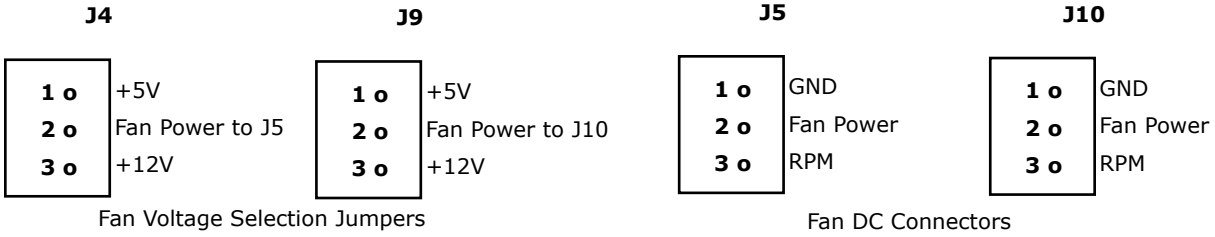
Jumper Reference

Drawings ONLY - for more detailed information on these parts, refer to the descriptions shown previously in this manual.



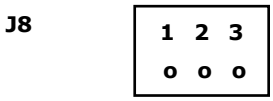
NOTE: The reference line to each component part has been drawn to Pin 1, where applicable. Pin 1 is also highlighted with a red square, where applicable.

Fan Speed / Power



Real-Time Clock/Calendar

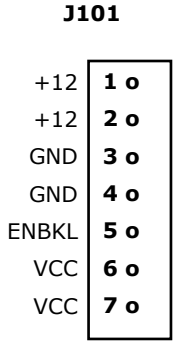
To reset board to factory default, remove the jumper from pins 1-2 on **J8** and place on pins 2-3 for 10 seconds. Replace the jumper on **J8** pins 1-2, power-up, and reconfigure the CMOS settings as desired.



CompactFlash

When using a CompactFlash device, Master/Slave mode selection can be accomplished by jumpering **J50**, shown below.

Panel Backlight Connection



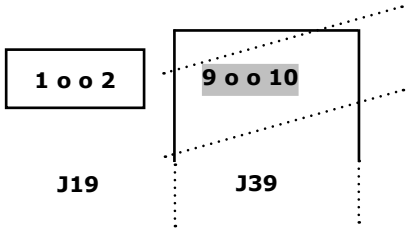
Flat Panel Power Selection

Panel power is selected by jumpering **J57**. There are two voltages available on the EBC-C3PLUS, +5 volts by jumpering **J57** 1-2, +3V by jumpering **J57** 2-3. Power is supplied to pins 49 and 50 of both **J36** and **J37**.

Watchdog Timer

The EBC-C3PLUS supports an internal timer with a period of 1.5 seconds with **J19** open, or 200 seconds with **J19** closed, will reset the CPU.

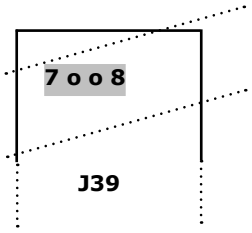
The watchdog timer powers-up disabled if **J39** pins 9-10 are closed, and must be enabled in software before timing will begin. If **J39** pins 9-10 are not jumpered, the watchdog is always enabled and petting must begin at once.



Digital I/O Enable

7-8 jumpered - the digital I/O is enabled at I/O address 120H

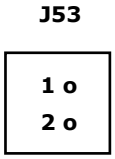
7-8 are open - the 16 addresses starting at I/O address 120H are free for use by other devices



Digital I/O VCC Enable

When **J53** is jumpered, +5V is provided at pin 49 of both **J41** and **J42**. It is the user's responsibility to limit current to a safe value (less than 400mA) to avoid damaging the CPU board.

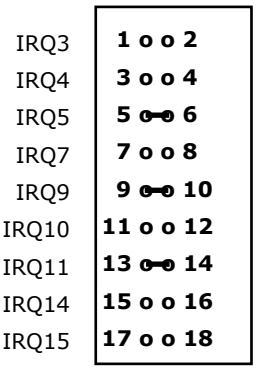
1-2 jumpered - +5V is provided at pin 49 of both J41 and J42



Interrupt Routing

All interrupts are routed to their respective PC/104 bus pins. On-board nonPnP peripherals are routed to their typical usage interrupts using the jumper block at **J52**.

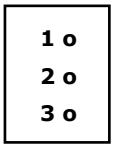
J52



IRQ3	1 o o 2	COM4
IRQ4	3 o o 4	COM3
IRQ5	5 o-o 6	DIGITAL I/O
IRQ7	7 o o 8	DIGITAL I/O
IRQ9	9 o-o 10	COM3
IRQ10	11 o o 12	DIGITAL I/O
IRQ11	13 o-o 14	COM4
IRQ14	15 o o 16	COM3
IRQ15	17 o o 18	COM4

Fan Speed / Power

J9



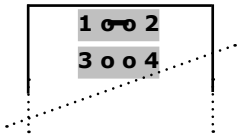
1 o +5V
2 o Fan Power to J9
3 o +12V

Fan Voltage Selection Jumpers

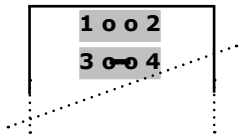
Silicon Disk Configuration

Silicon Disk Mode

J34



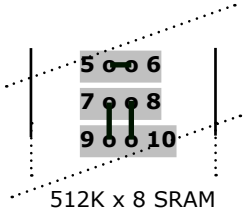
DOC usage



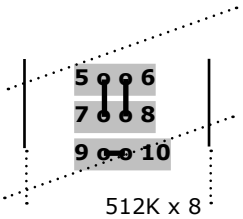
EPROM, SRAM, PEROM usage

Device Type Selection

J34

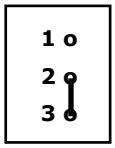


512K x 8 SRAM

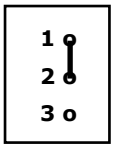


512K x 8
EPROM \ PEROM \ DiskOnChip usage

Battery Backup Selection



Normal Operation



Battery Backup Selected

NOTE: Having the jumper selected for battery backup when using anything other than low-power-standby SRAMs (such as EPROMs, or PEROMs) will result in the rapid draining of the on-board battery.

Silicon Disk Address Selection

The base address for the silicon disk can be selected by jumpering **J34** pins 11-18, as shown in the following chart.

J34 Base Address Selection Jumper				
Address	**17-18**	**15-16**	**13-14**	**11-12**
C800	X	X	open	X
CC00	X	X	open	open
D000	X	open	X	X
D400	X	open	X	open
D800	X	open	open	X
DC00	X	open	open	open

Serial Interface

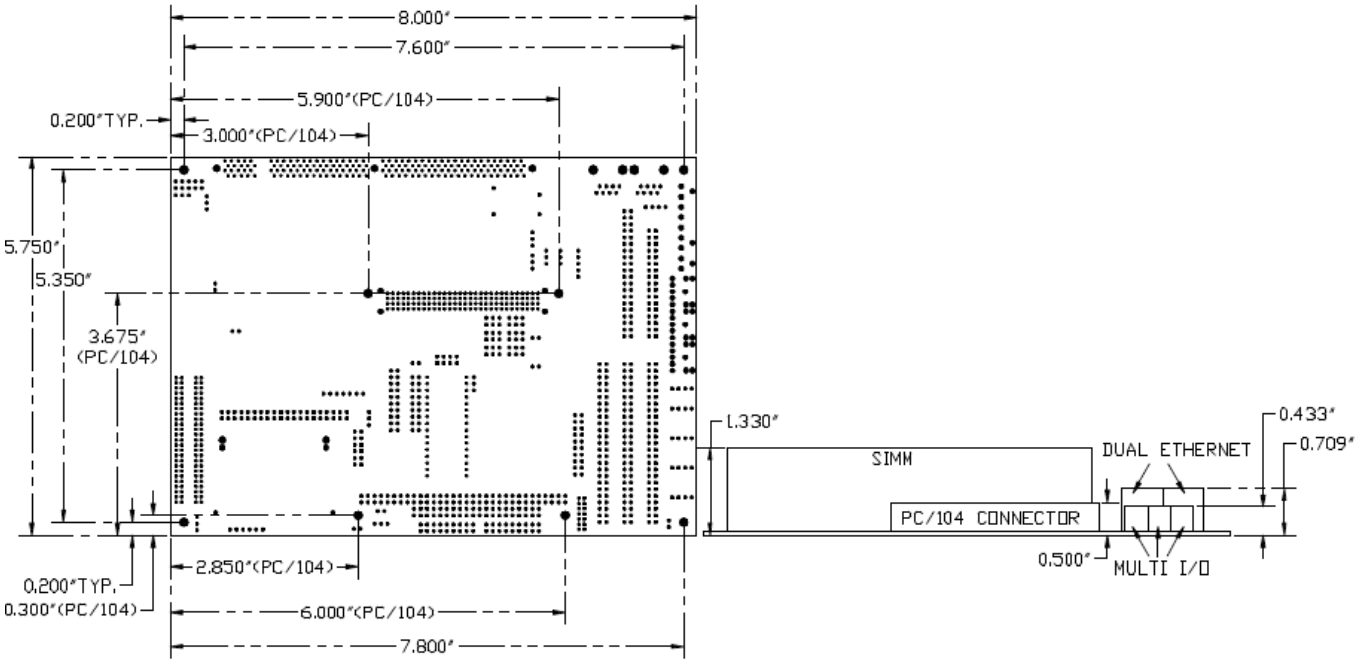
COM1 RS-232/RS-422/RS-485 Mode Selection - COM1 is configured using its specific jumper block. The table below shows the appropriate jumpering for the various modes.

Mode #	Description	J18	J21	Termination		
				J26	J23	J26
				TX(100)	RX(100)	TX/RX (300)
1	RS-232	1-2	Open	N/A	N/A	N/A
2	RS-422 RTS Enable	3-4	5-6	3-4	1-2	1-2 3-4 5-6
3	RS-422 Auto Enable	5-6 (one node must use TX/RX 300 Termination	5-6	N/A	1-2	1-2 3-4 5-6
4	RS-485 RTS Enable	3-4	1-2	3-4	N/A	1-2 3-4 5-6
5	RS-485 RTS Enable with Echo-Back	3-4	3-4	3-4	N/A	1-2 3-4 5-6
6	RS-485 Auto Enable	5-6 (one node must use TX/RX 300 Termination	1-2	3-4	N/A	1-2 3-4 5-6
7	RS-485 Auto Enable with Echo-Back	5-6 (one node must use TX/RX 300 Termination	3-4	N/A	N/A	1-2 3-4 5-6

COM2 RS-232/RS-422/RS-485 Mode Selection - COM2 is configured using its specific jumper block. The table below shows the appropriate jumpering for the various modes.

Mode #	Description	J17	J20	Termination		
				J25	J28	J26
				TX(100)	RX(100)	TX/RX (300)
1	RS-232	1-2	Open	N/A	N/A	N/A
2	RS-422 RTS Enable	3-4	5-6	3-4	1-2	1-2 3-4 5-6
3	RS-422 Auto Enable	5-6 (one node must use TX/RX 300 Termination	5-6	N/A	1-2	1-2 3-4 5-6
4	RS-485 RTS Enable	3-4	1-2	3-4	N/A	1-2 3-4 5-6
5	RS-485 RTS Enable with Echo-Back	3-4	3-4	3-4	N/A	1-2 3-4 5-6
6	RS-485 Auto Enable	5-6 (one node must use TX/RX 300 Termination	1-2	3-4	N/A	1-2 3-4 5-6
7	RS-485 Auto Enable with Echo-Back	5-6 (one node must use TX/RX 300 Termination	3-4	N/A	N/A	1-2 3-4 5-6

Mechanical Drawing



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE FRACTIONS ANGLES +/- 1/2° DECIMALS .XX ± .03 .XXX ± .010	CUSTOMER APPROVAL	DATE	WinSystems, Inc. "THE STD BUS AUTHORITY"
	APPROVAL	DATE	EBC-C3 MOUNTING DIMENSIONS
MACHINE FINISH ✓	CHECKER	DATE	SIZE C · CAGE CODE 1AU87 · DWG NO. EBCC3.DWG · REV A
	DRAFT/DESIGN M.BROWNING	DATE 10/07/03	SCALE · CAD ID: EBCC3.DWG · SHEET 1 OF 1

Specifications

Electrical

Bus Interface	:PC/104 16-bit expansion bus PC/104-*Plus* 32-bit expansion bus
System Clock	:Front-side Bus = 133 MHz
Interrupts	:TTL Level input
Power Requirements	:VCC+5V ± 5% at 3.4A typical with a VIA 1 GHz processor with 512 MB SDRAM installed. VCC +5V ± 5% at 3.1A typical with a VIA 733 MHz processor with 512 MB SDRAM installed.
VCC1	:+12V ± 5% (not required - PC/104 expansion or Flat Panel use only)
VCC2	:-12V ± 5% (not required - PC/104 expansion or Flat Panel use only)
VCC3	:+3.3V (not required – for PC/104-*Plus* expansion use only)

System Memory

Memory Socket	:168-pin 3.3V DIMM module; PC133 SDRAM Module
Memory Addressing	:512 MB
BIOS ROM	:256 KB Atmel Flash (reprogrammable on board)

Solid State Disk (SSD)

Capacity	:One (1) 32-pin, JEDEC socket supports 4 MB SRAM, 4 MB PEROM, 4 MB EPROM, 16 MB EPROM or the SanDisk 32-pin DiskOnChip®

Mechanical

Dimensions	: 5.75” x 8.0” x 0.60” (without PC/104 modules or cables)
Weight	: 3.0 oz

Connectors

Multi-I/O	:50-pin RN type IDH-50LP
Digital I/O	:Two (2), 50-pin RN type IDH-50LP
COM3/COM4	:20-pin RN type IDH-20LP
Floppy Disk	:34-pin RN type IDH-34-LP
CRT	:14-pin 2 mm Molex Type 87331-1420
Flat Panel	:Two (2), 50-pin 2 mm Molex Type 87331-5020
Power/Reset	:9-pin inline Molex type 26-60-7091
Fan Power	:3-pin inline Molex type 22-11-2032
Mouse	:5-pin inline latching Molex type 22-11-2052
USB	:Four (4), 4-pin inline latching Molex type 22-11-2042
PC/104-*Plus* Bus	:120-Pin SAMTEC type TS-30-Q
PC/104 Bus	:64-Pin SAMTEC type ESQ-132-12-G-D 40-Pin SAMTEC type ESQ-120-12-G-D
IDE	:40-pin 2mm Molex Type 70246-4021 44-pin STMM-122-02-G-D-SM-P-TR
Audio	:Three (3) 3.5 mm miniature stereo phone jacks
Ethernet	:Two (2) RJ-45

Environmental

Operating Temperature	:-40°C to +85°C
Noncondensing relative Humidity	:5% to 95%
MTBF	:7.3 yrs

WARRANTY REPAIR INFORMATION

WARRANTY

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WARRANTY SERVICE

1. To obtain service under this warranty, obtain a return authorization number. In the United States, contact the WinSystems' Service Center for a return authorization number. Outside the United States, contact your local sales agent for a return authorization number.

2. You must send the product postage prepaid and insured. You must enclose the products in an anti-static bag to protect from damage by static electricity. WinSystems is not responsible for damage to the product due to static electricity.