OPERATIONS MANUAL
SAT-DX

REVISION HISTORY

P/N 403-248-000

ECO Number	Date Code	Rev Level
ORIGINATED	961017	D
97-37	970602	D1
97-106	971110	D2
97-107	971110	D3
97-113	971117	E
98-16	980217	E1
98-31	981006	G
99-31	990721	H
99-84	001001	I
01-23	010425	I1

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1 GENERAL INFORMATION

1.1 FEATURES

- 80486DX4-100 Processor Selection
- 100% PC/AT Hardware/Software Compatibility
- Up to 64 MBytes of DRAM supported
- User installable SIMM DRAM modules or factory installed ruggedized DRAM
- Onboard Solid State Disk for EPROM, PEROM, SRAM or FLASH
- Industry Standard Award BIOS with POST
- Two 16550 Compatible UARTS with RS-232 and optional RS-422/RS-485 Support
- Bi-directional LPT port supports EPP and ECP modes
- 24 Multipurpose Digital I/O Lines
- Onboard Local Bus IDE interface
- Onboard Floppy Disk Controller
- 16-Bit PC/104 Bus Expansion
- Watchdog Timer with Powerfail/Brownout Monitoring
- Status and Hard Disk Activity LEDs
- 5 Volt Only Operation

1.2 GENERAL DESCRIPTION

The SAT-DX is a small, high-performance embeddable computer system on a single board. Its full PC/AT hardware complement and industry standard AWARD BIOS assures full hardware and software compatibility with PC software and operating systems. The SAT-DX includes onboard interfaces for floppy disks, IDE fixed disks, Parallel printer, and two serial channels with RS-232, RS-422, or RS-485 capability on either or both channels. A full 16-bit PC/104 expansion bus is provided for further expansion to an entire industry of add-on peripherals including high-speed VGA controllers, sound and speech modules, SCSI controllers, Analog I/O modules, and literally hundreds of other options available from WinSystems and a variety of vendors supporting the PC/104 standard. User installable/upgradeable 72-pin SIMM DRAM modules are supported up to a maximum of 64 Megabytes. Optional factory installed DRAM is also available for applications that may be intolerant to the limitations of the SIMM modules lack of ruggedness. An onboard Silicon Disk array supports disks of up to 2 Megabytes in size and can utilize SRAM, PEROM or EPROM as the disk media. Boot capability is provided onboard and a set of utilities and drivers are provided to make the silicon disk based system very user friendly. Alternately, the M-Systems' DiskOnChip FLASH modules may be populated, supporting disk sizes ranging from 2 Megabytes to 72 Megabytes.

1.3 Specifications

1.3.1 Electrical

Bus Interface : PC/104 8-Bit and 16-Bit expansion bus

System Clock : Jumper programmable from 4MHz to 50MHz

Interrupts : TTL Level input

VCC : +5V +/-5% at 1000mA typical with 486DX4-100 and 8MB DRAM

VCC1: +12V +/-5% (Not required. PC/104 Expansion Only)

VCC2: -12V +/-5% (Not Required. PC/104 Expansion Only)

1.3.2 Memory :

Addressing : 64 Megabyte addressing

BIOS ROM : 128K OTPROM

Memory SIMM Socket : 72-Pin Standard or EDO DRAM in sizes from 1M to 32M

SSD Memory : Two 32-pin JEDEC standard sockets support 4-MBit SRAM, 4-MBit PEROM, 4-MBit EPROM, 8-MBit EPROM or one M-Systems 32-pin DOC (DiskOnChip) Module.

1.3.3 Mechanical

Dimensions : 4.5 X 7.1 X .60 inches (without PC/104 modules or cables)

PC-Board : FR4 Epoxy Glass with 6 signal layers and 2 power planes with screened component legend, and plated through holes.

Jumpers : 0.025" square posts on 0.10" centers

Connectors :

Multi I/O:	50 pin RN type IDH-50-LP
RS-422/RS-485 :	10 Pin RN type IDH-10-LP
Floppy Disk :	34 Pin RN type IDH-34-LP
Fixed Disk :	40 pin RN type IDH-40-LP
PC/104 BUS :	64 pin SAMTECH type ESQ-132-12-G-D 40 pin SAMTECH type ESQ-120-12-G-D

Power/Reset Connector: 8 Pin Molex

1.3.4 Environmental

Operating Temperature : 0° to +60°C

NOTE : The operating temperature specification is highly dependent upon the type and speed of the CPU installed and any heat- sinking or cooling air flow supplied. The CPU case and junction temperature, as specified by the manufacturer, will be the limiting factors on this product.

Non-Condensing Humidity : 5 to 95%

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2 SAT-DX Technical Reference

2.1 Introduction

This section of the manual is intended to provide sufficient information regarding the configuration and usage of the SAT-DX board. WinSystems maintains a Technical Support group to help answer questions regarding configuration, usage, or programming of the board. For answers to questions not adequately addressed in this manual contact Technical Support at (817) 274-7553 between 8AM and 5PM Central Time.

2.2 Processor Selection

The SAT may be populated with any of a variety of 486 compatible processors from CYRIX, AMD, or INTEL. The CPUs are surface mount devices and are factory installed. There are no user configuration jumpers for CPU type. The following configuration table is provided for reference purposes.

Jumpering	S486DX2-66	S486DX4-100	AMD-X5-133S	AM486DE2-66	INTEL DX2-50
W15, 1-2	INSTALLED	OPEN	INSTALLED	INSTALLED	OPEN
W15, 2-3	OPEN	INSTALLED	OPEN	OPEN	OPEN
W11	INSTALLED	INSTALLED	INSTALLED	OPEN	OPEN
W12	INSTALLED	INSTALLED	INSTALLED	INSTALLED	OPEN
W21, 1-2	OPEN	OPEN	OPEN	OPEN	OPEN
W21, 2-3	INSTALLED	INSTALLED	INSTALLED	INSTALLED	INSTALLED
W19	INSTALLED	INSTALLED	INSTALLED	INSTALLED	INSTALLED
W14, 1-2	OPEN	OPEN	OPEN	INSTALLED	INSTALLED
W14, 2-3	INSTALLED	INSTALLED	INSTALLED	OPEN	OPEN
W10	OPEN	OPEN	OPEN	OPEN	OPEN
W20, 2-3	OPEN	OPEN	OPEN	OPEN	OPEN
W20, 1-2	INSTALLED	INSTALLED	INSTALLED	INSTALLED	OPEN
W13, 1-2	OPEN	OPEN	OPEN	OPEN	OPEN
W13, 2-3	INSTALLED	INSTALLED	INSTALLED	INSTALLED	OPEN

2.3 ALI 1487/1489 Chipset

The SAT-DX utilizes the ALI FINALI-486 Chipset which provides a highly integrated high-performance backbone for full PC/AT compatibility. The chipset contains the logic for DRAM and bus state control as well as the standard complement of 'AT' class peripherals internally, including :

8 DMA Channels compatible with PC-AT 8237A DMA Controllers

15 Interrupt inputs compatible with master/slaved 8259 interrupt controllers

Three 8254 compatible timer/counter channels

A PC-AT compatible real time clock/calendar with CMOS RAM

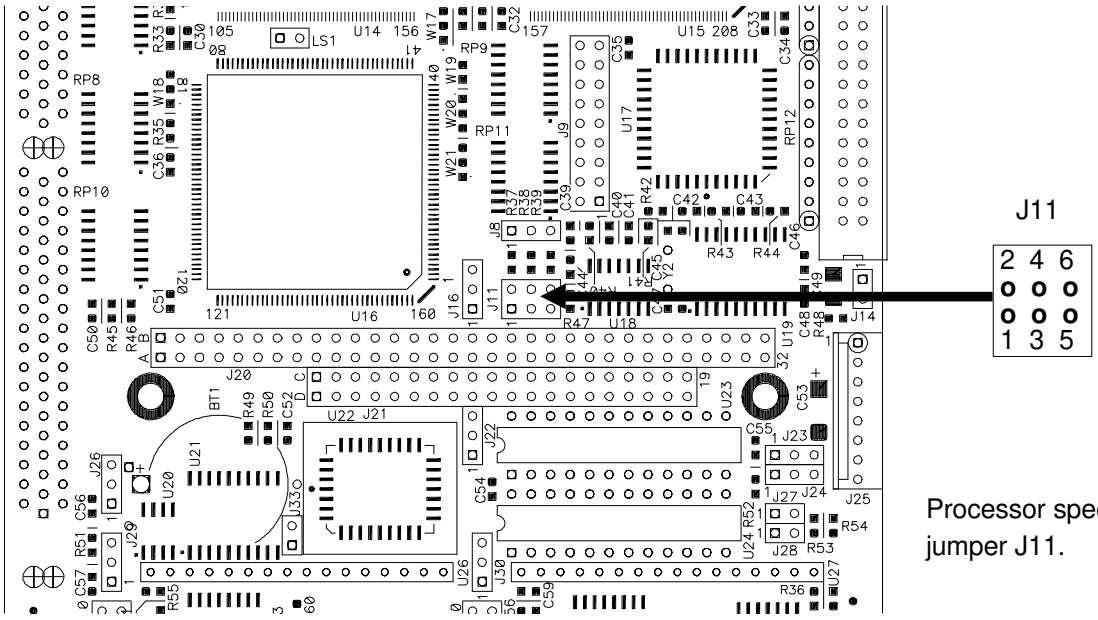
A Local BUS IDE interface

A PC-AT compatible Keyboard interface

The functional units are 100% PC-AT compatible and are supported by the AWARD BIOS and Setup. Users desiring to access these internal peripherals directly should refer to any manufacturer's generic literature on the equivalent discrete component.

There are a number of internal registers within the Finali-486 Chipset that are used by the BIOS for control and configuration. Refer to the I/O Map in Appendix A for port usage to avoid conflicts when adding external I/O devices.

2.4 Processor Speed Selection



Processor speed select jumper J11.

The SAT-DX uses a crystal controlled frequency synthesizer to control the CPU clock rate. The jumper block at J11 allows for the selection of any of 8 CPU clock frequencies ranging from 4Mhz to 50Mhz. The table below gives all of the possible CPU clock speeds available.

Speed Select Jumper J11			
CPU Speed	Pins 1-2	Pins 3-4	Pins 5-6
4MHz	ON	ON	ON
8MHz	OFF	ON	ON
16MHz	ON	OFF	ON
20MHz	OFF	OFF	ON
25MHz	ON	ON	OFF
33MHz	OFF	ON	OFF
40MHz	ON	OFF	OFF
50MHz	OFF	OFF	OFF

NOTE : The SAT-DX board will be jumpered at the factory for the rated speed of the installed processor. Jumpering J11 to any speed in excess of the rated speed may result in CPU overheating, misoperation, and possible destruction of the CPU. Failures of CPUs which have been exposed to frequencies above their rated speed or to temperatures above their rated value will not be covered under the WinSystems standard product warranty.

2.5 Memory Installation Selection

The SAT-DX utilizes DRAM memory in one of two forms, either 72-pin standard SIMM modules in sizes of 1 Megabyte to 64 Megabytes are usable or factory installed SMT memory in sizes of 4, 8, 16, or 32 Megabytes.

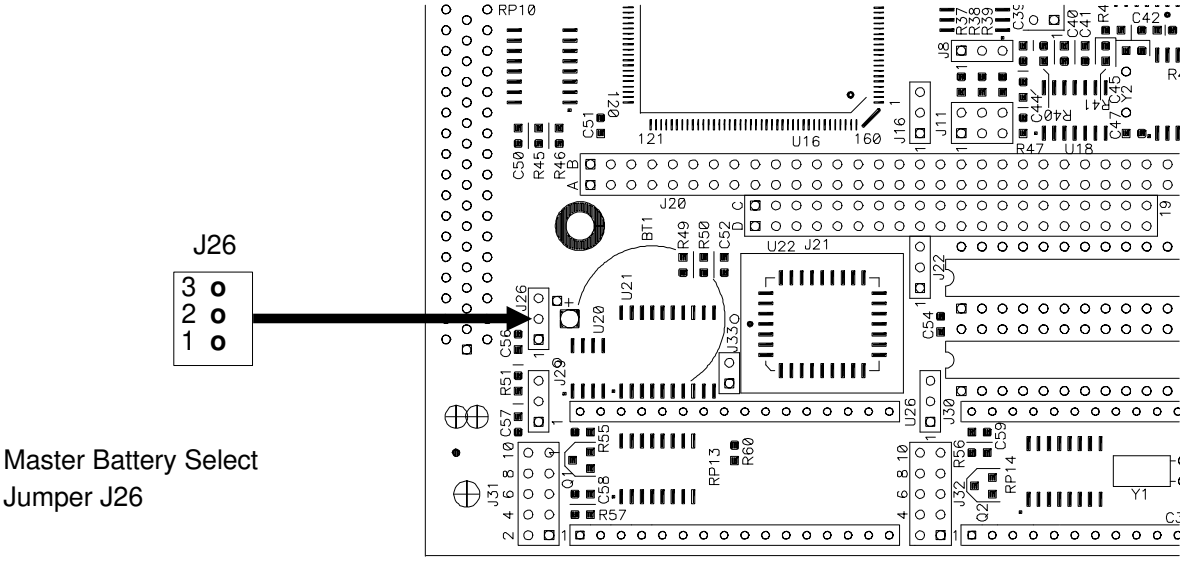
When no factory DRAM is provided, the SAT-DX allows for user installation of standard 72-pin (32-bit wide) SIMM DRAM modules in 70nS or 60nS speeds. These are the standard SIMM modules used in most 32-bit 386 and 486 based desktop personal computers. These memory modules range in size from 1 Megabyte to 64 Megabytes in size.

Go to **http://www.winsystems.com/memory** for a list of qualified modules.

Installation is accomplished with power off by angling the SIMM module approximately 30 degrees from horizontal and inserting the fingers into the connector. The SIMM module is keyed slightly off-center and cannot be inserted backwards without extreme force. Once the fingers are in the socket the module is then rotated to the horizontal until the retaining clips snap into place. Removal is the reverse process. Pull the retaining clips outward and the SIMM module once released should rotate back to an appropriate removal angle.

SIMM modules should not be removed and reinserted any more often than necessary as the connectors were not designed for repeated use and intermittent operation may result because of insufficient contact or retaining force.

2.6 Real Time Clock Calendar



The SAT-DX contains an onboard Clock/Calendar within the ALI 1487 chip. This clock is fully compatible with the MC146818A used in the original PC-AT computers. This clock has a number of features including periodic and alarm interrupt capabilities. In addition to the Time and Date keeping functions the system configuration is kept in CMOS RAM contained within the clock section. This RAM holds all of the setup information regarding hard and floppy disk types, video type, shadowing, wait states, etc. Refer to the section on the Award BIOS Setup for complete information on what is configured via the CMOS RAM.

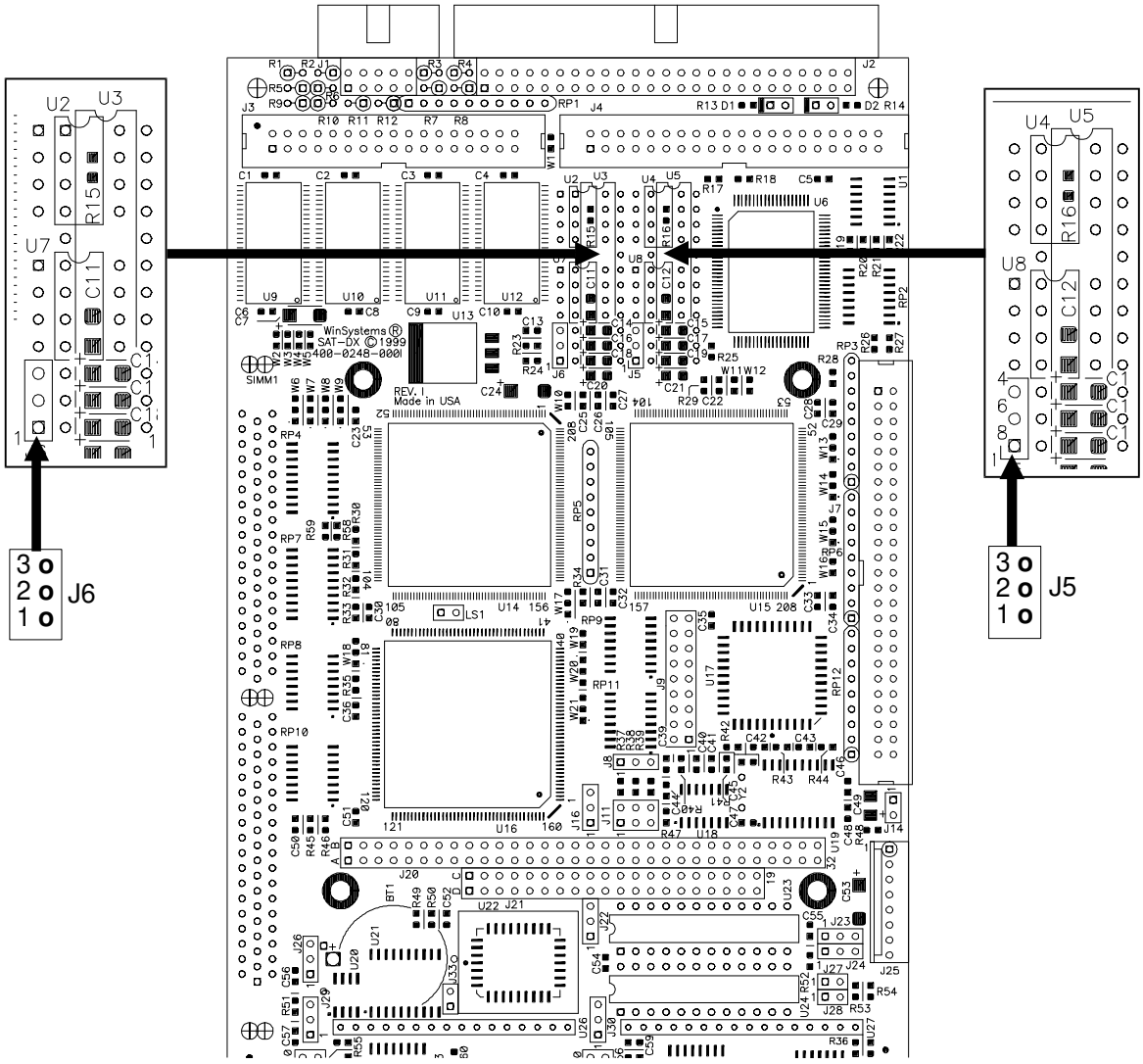
It may become necessary at some time to make the CMOS RAM forget its current configuration and to start fresh with factory defaults. This may be accomplished by removing power and the board from the system. Then remove the jumper from J26 pins 1-2 and place it on J26 pins 2-3 for approximately 10 seconds. Replace the jumper to its original position on pins 1-2, reinstall the board, power up, and reconfigure the CMOS setup as desired.

2.7 Keyboard Interface

The SAT-DX contains an onboard PC-AT style keyboard controller. Connection is made through the multi-I/O connector at J2. An adapter cable P/N CBL-162-1 is available from WinSystems to make ready access to all of the devices terminated at the multi-I/O connector. Users desiring custom connections should refer to the multi-I/O connector pin definitions given later in this manual.

2.8 Serial Interface

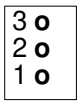
The SAT-DX provides two RS-232 serial channels onboard, configurable as RS-422 or RS-485 with the addition of optional driver ICs. The configuration options for each of the supported modes are shown on the following pages.



2.8.1 COM 1 - RS-232

Jumper Position

J6

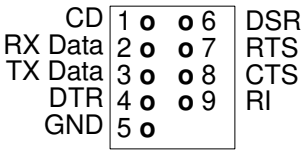


Driver IC Status

U2 - Not Installed
U3 - Installed
U7 - Not Installed

I/O Connector Pin

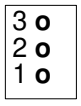
COM1 DB9



2.8.2 COM 2 - RS-232

Jumper Position

J5

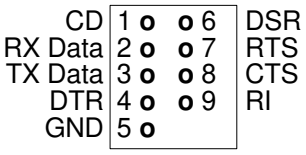


Driver IC Status

U4 - Not Installed
U5 - Installed
U8 - Not Installed

I/O Connector Pin

COM2 DB9



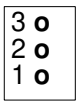
2.8.3 RS-422 Mode Configuration

RS-422 Signal levels are supported on either or both serial channels with the installation of the optional "Chip Kit" WinSystems' part number CK-75176-2. This kit provides the driver ICs necessary for a single channel of RS-422. If two channels of RS- 422 are required then two kits will be needed. RS-422 is a 4-wire point to point full-duplex interface allowing much longer cable runs than are possible than with RS-232. The differential transmitter and receiver twisted-pairs offer a high degree of noise immunity. RS-422 usually requires that the lines be terminated at both ends. This termination can be accomplished either on the cable or by installing resistors on the board in locations reserved for them. The methodology for determining the correct resistor values is beyond the scope of this document but it is recommended the trial values of 100 ohms be used in all three locations at the receiver end. The following illustrations show the correct jumpering, driver IC installation, I/O connector pin definitions, and termination resistor locations for each of the channels when used in RS-422 mode.

2.8.4 COM 1 - RS-422

Jumper Position

J6

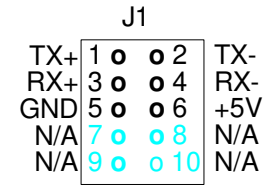


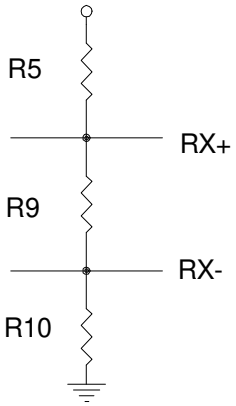
Driver IC Status

U2 - Installed
U3 - Not Installed
U7 - Installed

I/O Connector Pin

J1



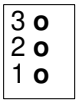


RS-422 NOTE : When used in RS-422 mode, the transmitter must be enabled by setting the RTS bit in the Modem Control Register (Bit 1).

2.8.5 COM 2 - RS-422

Jumper Position

J5

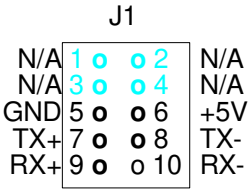


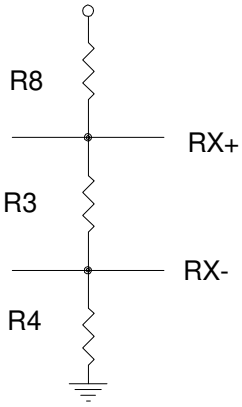
Driver IC Status

U4 - Installed
U5 - Not Installed
U8 - Installed

I/O Connector Pin

J1





RS4-22 NOTE : When used in RS-422 mode, the transmitter must be enabled by setting the RTS bit in the Modem Control Register (Bit 1).

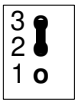
2.8.6 RS-485 Mode Configuration

The RS-485 multi-drop interface is supported on both serial channels with the installation of the optional "Chip Kit" WinSystems' part number CK-75176-2. A single kit is sufficient to configure both channels for RS-485. RS-485 is a 2-wire multi-drop interface where only one station at a time talks (transmits) while all others listen (receive). RS-485 usually requires the twisted line-pair be terminated at each end of the run. The required termination values are dependent upon a number of factors including: line impedance, line length, etc. A good trial value is 100 ohm resistors in all three locations. The following illustrations show the correct jumpering, driver IC installation, I/O connector pin-out, and termination resistor locations for each of the channels when used is RS-485 mode.

2.8.7 COM 1 - RS-485

Jumper Position

J6



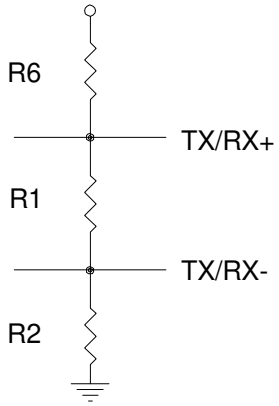
Driver IC Status

U2 - Installed
U3 - Not Installed
U7 - Not Installed

I/O Connector Pin

J1

TX/RX+	1	2	TX/RX-
N/A	3	4	N/A
GND	5	6	+5V
N/A	7	8	N/A
N/A	9	10	N/A

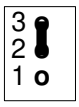


RS485 NOTE : Because RS-485 uses a single twisted-pair, all transmitters are connected in parallel. Only one station may transmit, or have its transmitter enabled at a time. The transmitter Enable/Disable is controlled by bit 1 in the Modem Control Register (RTS). When set, the transmitter is enabled, when cleared (the normal state) the transmitter is disabled and the receiver is enabled. Note that it is necessary to allow some minimal settling time after enabling the transmitter before transmitting the first character. Likewise, following a transmission, it is necessary to be sure that all characters have been completely shifted out of the UART (Check Bit 6 in the Line Status Register) before disabling the transmitter to avoid chopping off the last character.

2.8.8 COM 2 - RS-485

Jumper Position

J5

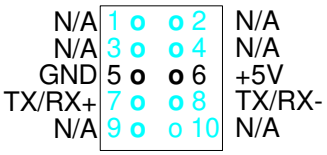


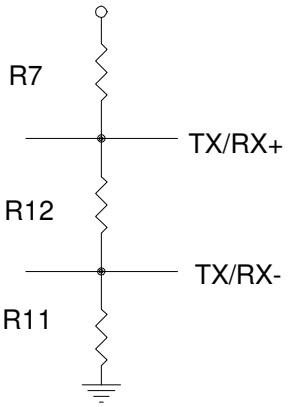
Driver IC Status

U4 - Installed
U5 - Not Installed
U8 - Not Installed

I/O Connector Pin

J1





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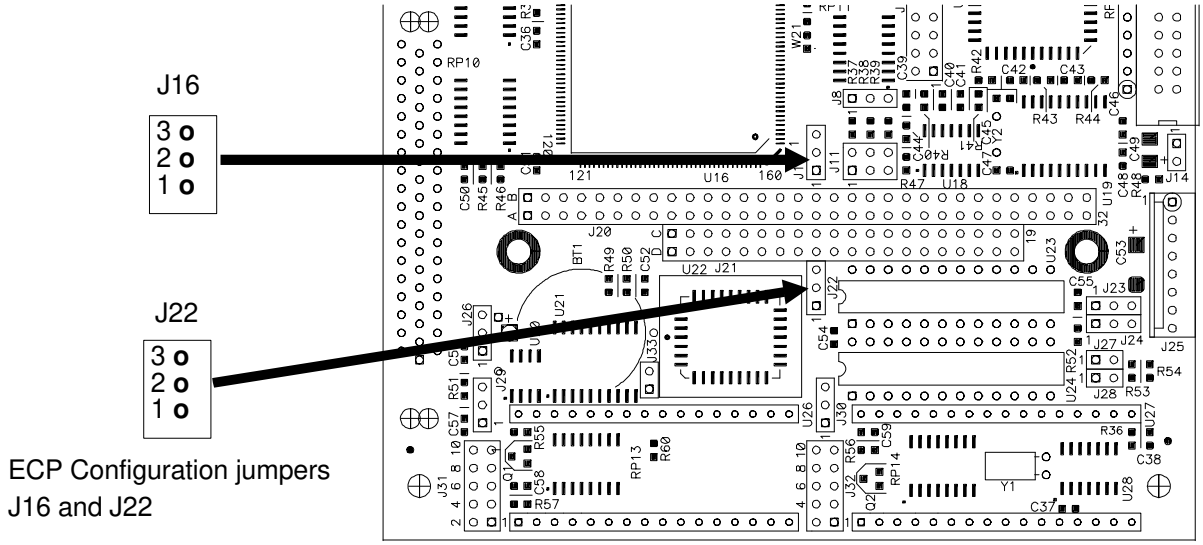
2.9 Parallel Printer Interface



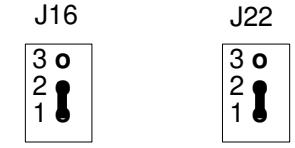
ECP Configuration jumpers
J16 and J22

The SAT-DX supports a fully bi-directional parallel printer port capable of EPP and ECP operations. The parallel port is I/O mapped at 278H and is terminated at the multi-I/O connector J2. The pin definitions for the parallel port connector DB-25 when used with the CBL-162-1 cable is as shown below :

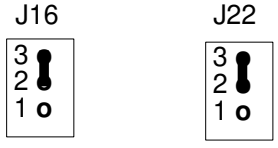
STROBE	1 o o 14	AUTOFD
PD0	2 o o 15	ERROR
PD1	3 o o 16	INIT
PD2	4 o o 17	SLIN
PD3	5 o o 18	GND
PD4	6 o o 19	GND
PD5	7 o o 20	GND
PD6	8 o o 21	GND
PD7	9 o o 22	GND
ACK	10 o o 23	GND
BUSY	11 o o 24	GND
PE	12 o o 25	GND
SLCT	13 o	

2.9.1 ECP DMA Configuration

When the Parallel port is used in an ECP configuration, J16 and J22 are used to configure the DMA channel to be used for ECP transfers. DMA Channel 1 or Channel 3 is selectable as shown below :



DMA Channel 1 Select



DMA Channel 3 Select

2.10 Speaker/Sound Interface

The SAT-DX utilizes a high-impedance piezo type device for audio output. BIOS Beep codes, error signaling, or user defined tones can be presented via this device.

2.11 PC/104 Bus interface

The SAT-DX supports I/O expansion through the standard PC/104 connectors at J20 and J21. The SAT-DX supports both 8-bit and 16-bit PC/104 modules. The PC/104 connector pin definitions are provided here for reference purposes.

J20

GND	B1	o o	A1	IOCHK
RESET	B2	o o	A2	BD7
+5V	B3	o o	A3	BD6
IRQ9	B4	o o	A4	BD5
-5V	B5	o o	A5	BD4
DRQ2	B6	o o	A6	BD3
-12V	B7	o o	A7	BD2
0WS	B8	o o	A8	BD1
+12V	B9	o o	A9	BD0
GND	B10	o o	A10	IOCHRDY
MEMW	B11	o o	A11	AEN
MEMR	B12	o o	A12	SA19
IOW	B13	o o	A13	SA18
IOR	B14	o o	A14	SA17
DACK3	B15	o o	A15	SA16
DRQ3	B16	o o	A16	SA15
DACK1	B17	o o	A17	SA14
DRQ1	B18	o o	A18	SA13
REFRESH	B19	o o	A19	SA12
SYSCLK	B20	o o	A20	SA11
IRQ7	B21	o o	A21	SA10
IRQ6	B22	o o	A22	SA9
IRQ5	B23	o o	A23	SA8
IRQ4	B24	o o	A24	SA7
IRQ3	B25	o o	A25	SA6
DACK2	B26	o o	A26	SA5
TC	B27	o o	A27	SA4
BALE	B28	o o	A28	SA3
+5V	B29	o o	A29	SA2
OSC	B30	o o	A30	SA1
GND	B31	o o	A31	SA0
GND	B32	o o	A32	GND

J21

GND	C0	o o	D0	GND
SBHE	C1	o o	D1	MEMCS16
LA23	C2	o o	D2	IOCS16
LA22	C3	o o	D3	IRQ10
LA21	C4	o o	D4	IRQ11
LA20	C5	o o	D5	IRQ12
LA19	C6	o o	D6	IRQ15
LA18	C7	o o	D7	IRQ14
LA17	C8	o o	D8	DACK0
MEMR	C9	o o	D9	DRQ0
MEMW	C10	o o	D10	DACK5
SD8	C11	o o	D11	DRQ5
SD9	C12	o o	D12	DACK6
SD10	C13	o o	D13	DRQ6
SD11	C14	o o	D14	DACK7
SD12	C15	o o	D15	DRQ7
SD13	C16	o o	D16	VCC
SD14	C17	o o	D17	MASTER
SD15	C18	o o	D18	GND
KEY	C19	o o	D19	GND

2.12 Floppy Disk Interface

The SAT-DX supports up to 2 standard 3 1/2" or 5 1/4" PC compatible floppy disk drives. The drives are connected via the I/O connector at J3. Note that the interconnect cable to the drives is a standard floppy I/O cable used on desk-top PCs. The cable must have the twisted section prior to the drive A: position. The pin definitions for the J3 connector are shown here for reference.

J3

GND	1	2		RPM/LC
GND	3	4		N/C
GND	5	6		N/C
GND	7	8		INDEX
GND	9	10		MTR0
GND	11	12		DRV1
GND	13	14		DRV0
GND	15	16		MTR1
GND	17	18		DIR
GND	19	20		STEP
GND	21	22		WDATA
GND	23	24		WGATE
GND	25	26		TRK0
GND	27	28		WPRT
GND	29	30		RDATA
GND	31	32		HDSEL
GND	33	34		DSKCHG

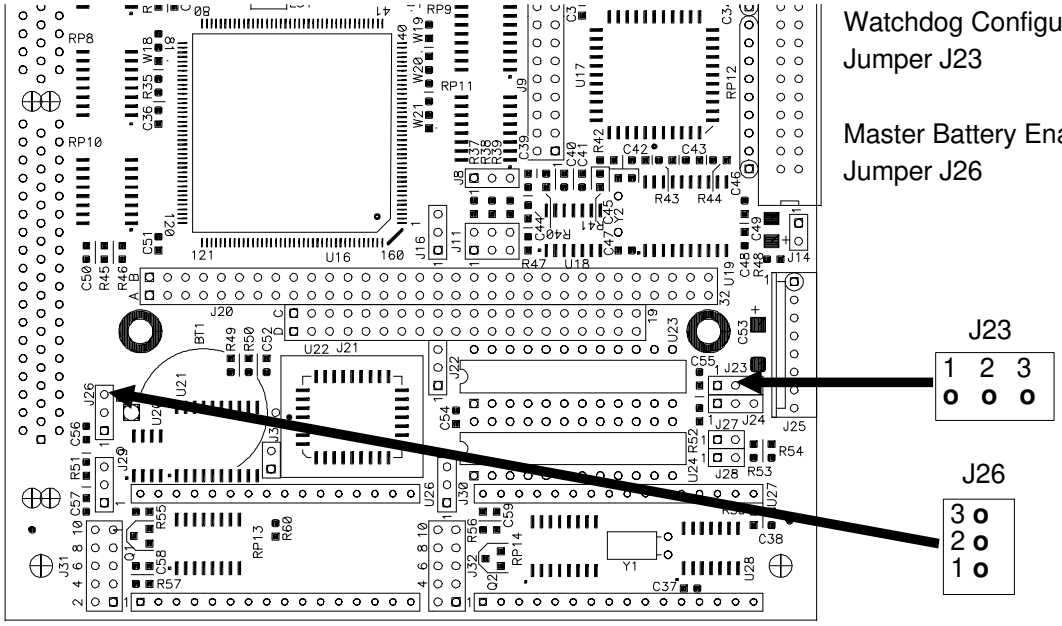
2.13 IDE Hard Disk Interface

The SAT-DX supports standard IDE fixed disks through the I/O connector at J4. A Red activity LED is present at D2. The pin definitions for the J4 connector are shown here :

J4

RESET	1	2		GND
D7	3	4		D8
D6	5	6		D9
D5	7	8		D10
D4	9	10		D11
D3	11	12		D12
D2	13	14		D13
D1	15	16		D14
D0	17	18		D15
GND	19	20		N/C
GND	21	22		GND
IOW	23	24		GND
IOR	25	26		GND
N/C	27	28		ALE
N/C	29	30		GND
INTRQ	31	32		IOCS16
A1	33	34		N/C
A0	35	36		A2
HDCS0	37	38		HDCS1
N/C	39	40		GND

2.14 Watchdog Timer Configuration



The SAT-DX board features a power-on voltage detect and a power-down/power brown-out reset circuit to protect memory and I/O from faulty CPU operation during periods of illegal voltage levels. This supervisory circuitry also features a watchdog timer which can be used to guard against software lockups. An internal self- timer with a period of 1.5 seconds will, when enabled, reset the CPU is the watchdog has not been serviced (petted) within the allotted time. There are three watchdog operational modes available on the SAT-DX. With no jumper installed on J23, the watchdog is totally disabled and can never reset the CPU. When J23 is jumpered pins 2-3, the watchdog circuit is permanently enabled and timing begins immediately with power-on. This mode is NOT compatible with the Award BIOS or with MS-DOS, but is available for directly embedded code that takes the place of the BIOS. The watchdog must be accessed at least every 1.5 seconds or a reset will occur. Petting in this mode is accomplished by writing to I/O port 1D0H with an alternating 1 and 0 value.

The alternate mode of operation is via software enable/disable control. This mode is set by jumpering J23, pins 1-2. In this mode the watchdog timer powers-up disabled and must be enabled in software before timing will begin. Enabling is accomplished by writing a 1 to I/O port 1D0H. Writing a 0 to I/O port 1D0H will disable the watchdog. After enabling the watchdog must be serviced at least every 1.5 seconds or a reset will occur. The petting is accomplished in either of 2 ways. The first method is to read port 1D8H and XOR the value read with 1 and rewrite the result to I/O port 1D8H. The second method is to do two consecutive writes to port 1D8H with a value of 0 followed by a value of 1. This mode of operation can be used with the BIOS and DOS provided that the watchdog is disabled before making any extensive BIOS or DOS calls, especially video or Disk I/O calls, which in some cases could exceed the 1.5 seconds allowed. The drawback to this mode is that a lockup dur-

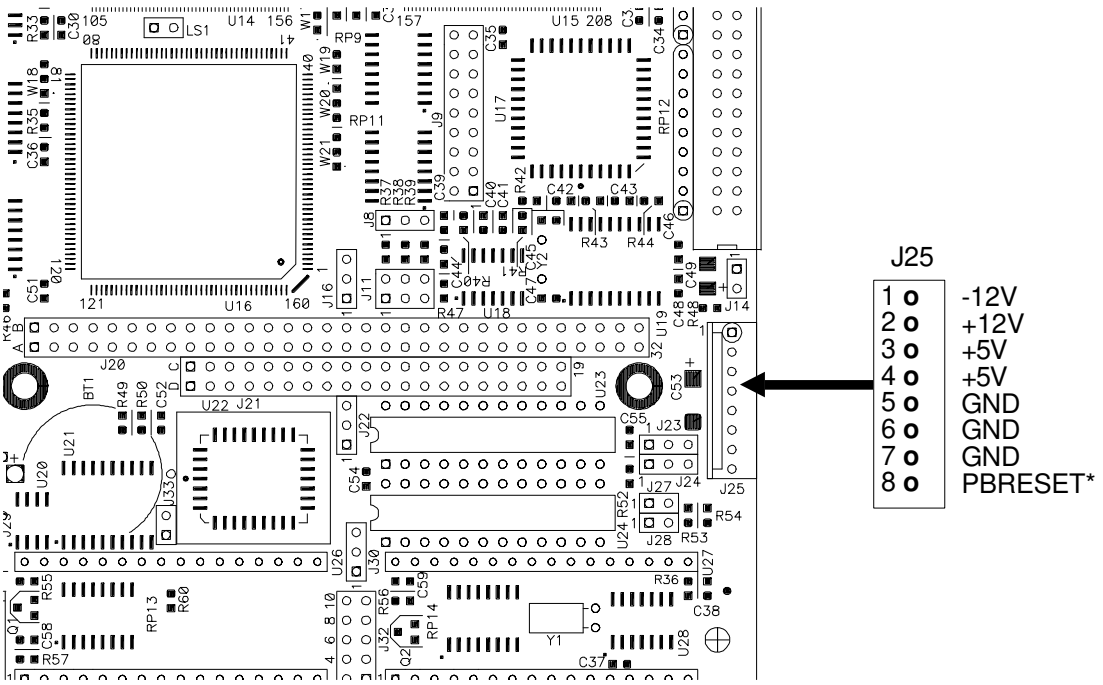
ing the time the watchdog is disabled will not allow for auto-recovery but will require an external source for a reset.

2.15 Battery Select Control

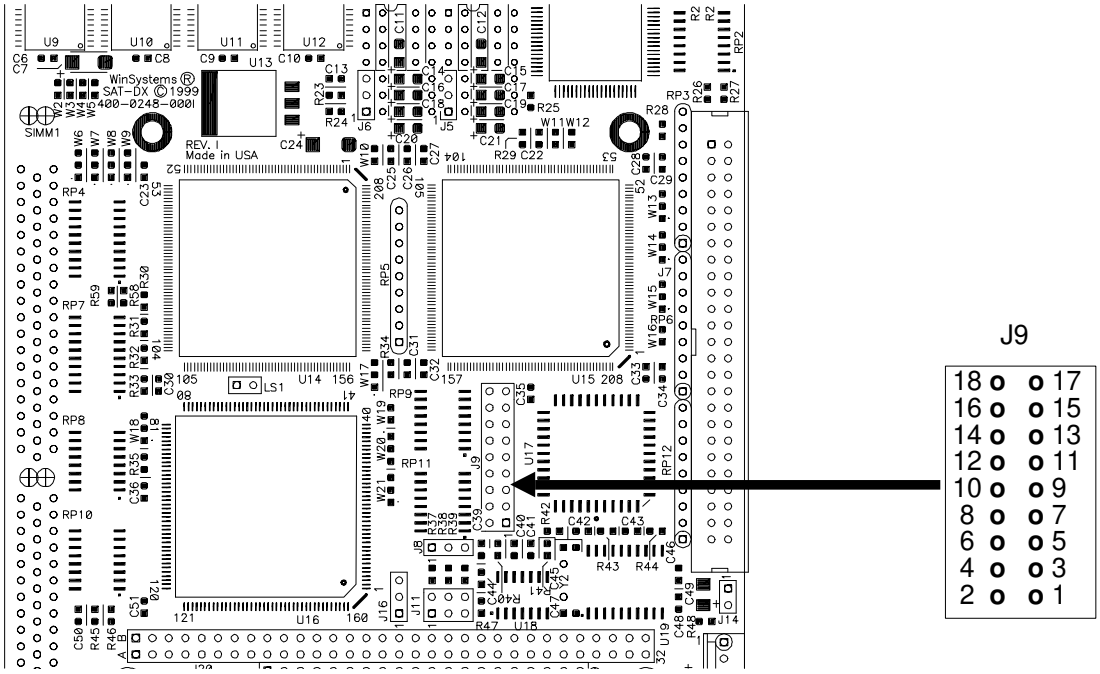
The SAT-DX has an onboard lithium battery used to sustain the Clock/Calendar CMOS setup information, and Solid State Disk information when SRAMs are used. A master battery enable jumper is provided at J26. With J26 jumpered pins 2-3 the battery is totally disconnected and no battery voltage is supplied to any circuitry on the board. Individual sockets in the Solid State Disk array may be jumpered for battery backup when using SRAMs if desired. Refer to the Silicon Disk Configuration section of this manual for details. It may become necessary or desirable at some time to erase the CMOS setup information due to incorrect or undesirable settings which are causing an inability to execute the setup utility or improper operation. To reset the CMOS memory to factory defaults, move the jumper from J26 pins 1-2 and place the jumper on J26 pins 2-3 for at least 10 seconds and then restore the jumper to the normal position on pins 1-2. This should result in the BIOS restoring defaults and prompting for setup during the next boot. Refer to section 3: Award BIOS Configuration for setup options and details.

2.16 Power/Reset Connections

Power is applied to the SAT-DX via the connector at J25. The pin definitions for J25 are given below. An optional push-button-reset may also be routed into J25 if desired.



2.17 Interrupt Routing

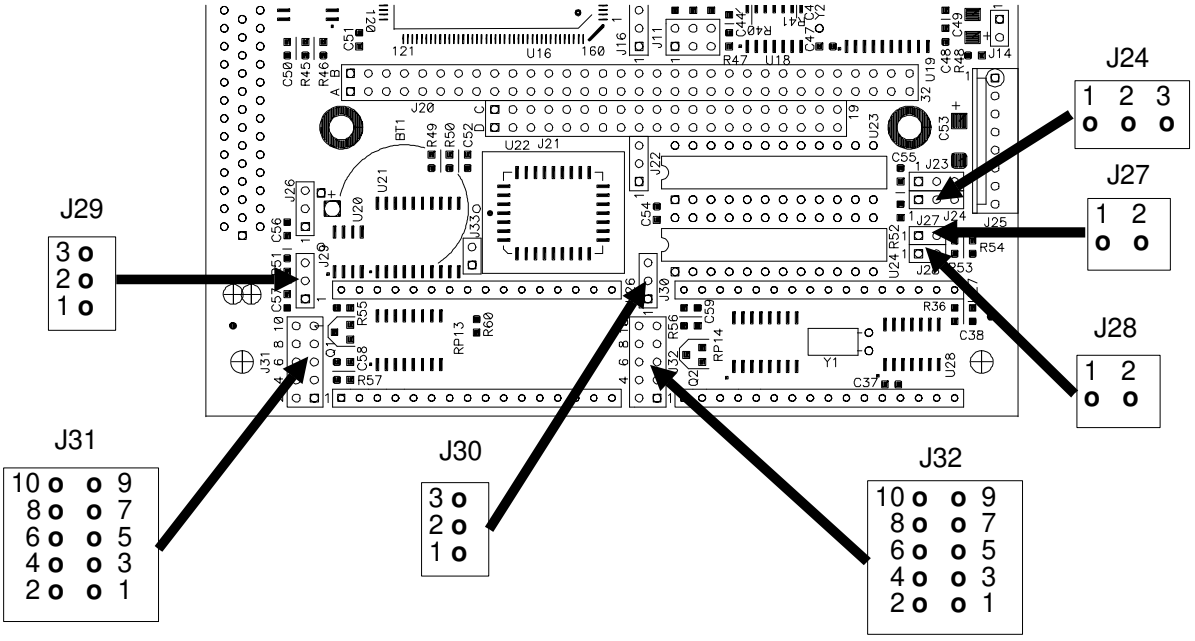


All interrupt inputs are routed to their respective PC/104 bus pins as shown earlier in the PC/104 bus interface section. Onboard peripherals, Serial, Parallel, and Disk are routed to their typical interrupt inputs using the jumper block at J9. This block allows disconnecting or rerouting of the onboard interrupts. The layout of the J9 jumper block is shown here, along with its default settings :

J9

IRQ14	18	17	HD Interrupt
IRQ9	16 o	o 15	COM2
IRQ3	14	13	COM2
IRQ4	12	11	COM1
IRQ5	10 o	o 9	FLOPPY
IRQ6	8	7	FLOPPY
IRQ7	6	5	LPT
IRQ7	4 o	o 3	8255 Port C - 0
NMI	2 o	o 1	8255 Port C - 3

2.18 Silicon Disk Configuration



The SAT-DX supports the use of EPROM, PEROM (Flash), SRAM, and the M-Systems' DiskOnChip (DOC) devices to be used as one or more Solid State Disk drives. Section 4 of this manual provides the necessary information for the generation and usage of the Silicon drives. This section documents the required hardware configurations for the various types of devices. The two 32-pin JEDEC memory sockets at U26 and U27 are used to contain the RAM, ROM, FLASH, or DOC devices used for the disk. The silicon disk array is memory mapped into a 16K byte hole at segment E400H and has an I/O control register at 1D4H.

2.18.1 Silicon Disk Mode

There are two basic modes of Silicon Disk operation available on the SAT-DX. The first uses the onboard BIOS extension and supports the use of 512K or 1M EPROMS, 512K SRAMs, or 512K ATMEL Flash devices. The second mode uses the M-Systems' DiskOn-Chip device. The mode is controlled via the jumper block at J28 as shown here :

SRAM, PEROM, EPROM USAGE

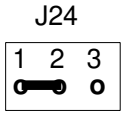
DISK-ON-CHIP USAGE

Note : Jumpering for DOC mode with EPROMs, RAMs, or FLASH devices installed effectively acts to disable the Solid State Disk and similarly when a DOC device is installed and the jumper is selected for standard devices the DOC is disabled.

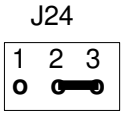
2.18.2 Device Size Selection

The onboard Solid State Disk array supports either 512K EPROMs, SRAMs, or FLASH devices or 1M EPROM devices. The device size selection is made at J24 as shown here :

NOTE : The device size jumper setting is irrelevant in the DOC mode.



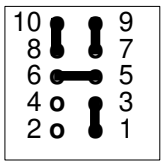
512K DEVICES



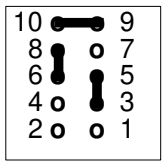
1MEG DEVICES

2.18.3 Device Type Selection

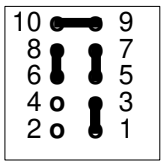
Each of the sockets in the array also has an individual device type jumper block at the device socket. J31 sets the device type for U26 and J32 sets the device type for U27. The supported device type jumperings are shown here :



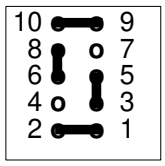
512K X 8 SRAM



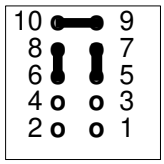
512K X 8 EPROM



512K X 8 PEROM



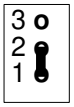
1MEG X 8 EPROM



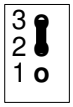
DOC DEVICE

2.18.4 Battery Backup Selection

When using SRAM devices and nonvolatile operation is desired, battery backup can be selected on a socket by socket basis. J30 for U27 and J29 for U26. The illustration below shows the jumpering for battery backup or standard operation.



Battery Backup
Enabled



Battery Backup
Disabled

NOTE : Having the jumper(s) selected for battery backup when using other than low-power-standby SRAMs (such as with EPROMs, or PEROMs) will result in the quick draining of the onboard battery.

2.18.5 Write Protect Control

When using SRAM or PEROM devices the jumper block at J27 can be used as a hardware write-protect. With J27 installed the BIOS will not allow writes to the disk array. Note that this jumper has no effect on DOC operations.

2.18.6 Silicon Disk Notes

1. When installing devices, U27 is the first device in the array and must always contain the first device of a bootable disk including the DiskOnChip option.

2. The DiskOnChip option must use the socket at U27. When a DOC is installed U26 is not usable for any purpose.

2.19 Parallel I/O

The SAT-DX contains an 8255 type device supporting 24 line of digital I/O. These 24 lines are terminated at J7. The base I/O address of the 8255 is 50H. refer to Appendix F for programming information on the 8255. The pin definitions for the J7 connector are shown here :

J7

Port C Bit 7	1 o	o 2	GND
Port C Bit 6	3 o	o 4	GND
Port C Bit 5	5 o	o 6	GND
Port C Bit 4	7 o	o 8	GND
Port C Bit 3	9 o	o 10	GND
Port C Bit 2	11 o	o 12	GND
Port C Bit 1	13 o	o 14	GND
Port C Bit 0	15 o	o 16	GND
Port B Bit 7	17 o	o 18	GND
Port B Bit 6	19 o	o 20	GND
Port B Bit 5	21 o	o 22	GND
Port B Bit 4	23 o	o 24	GND
Port B Bit 3	25 o	o 26	GND
Port B Bit 2	27 o	o 28	GND
Port B Bit 1	29 o	o 30	GND
Port B Bit 0	31 o	o 32	GND
Port A Bit 7	33 o	o 34	GND
Port A Bit 6	35 o	o 36	GND
Port A Bit 5	37 o	o 38	GND
Port A Bit 4	39 o	o 40	GND
Port A Bit 3	41 o	o 42	GND
Port A Bit 2	43 o	o 44	GND
Port A Bit 1	45 o	o 46	GND
Port A Bit 0	47 o	o 48	GND
+5V*	49 o	o 50	GND

***NOTE :** Pin 49 of J7 may be configured to supply + 5 Volts to pin 49 by placing a jumper on J14. The current draw from pin 49 should not exceed 300mA.

2.20 I/O Connector

The I/O to the serial channels, the printer port, and keyboard are all terminated via the connector at J2. An adapter cable part number CBL-162-1 is available from WinSystems to adapt to the conventional I/O connectors. The pin-out for J2 is shown here :

J2

COM1 - DCD	1	2	COM1 - DSR
COM1 - RXD	3	4	COM1 - RTS
COM1 - TXD	5	6	COM1 - CTS
COM1 - DTR	7	8	COM1 - RI
COM1 - GND	9	10	COM2 - DCD
COM2 - DSR	11	12	COM2 - RSX
COM2 - RTS	13	14	COM2 - TXD
COM2 - CTS	15	16	COM2 - DTR
COM2 - RI	17	18	COM2 - GND
LPT - STROBE	19	20	LPT - AUTOFD
LPT - PD0	21	22	LPT - ERROR
LPT - PD1	23	24	LPT - INIT
LPT - PD2	25	26	LPT - SLCTIN
LPT - PD3	27	28	LPT - GND
LPT - PD4	29	30	LPT - GND
LPT - PD5	31	32	LPT - GND
LPT - PD6	33	34	LPT - GND
LPT - PD7	35	36	LPT - GND
LPT - ACK	37	38	LPT - GND
LPT - BUSY	39	40	LPT - GND
LPT - PE	41	42	LPT - GND
LPT - SLCT	43	44	KEYBD - GND
KEYBD - GND	45	46	KEYBD - GND
KEYBD - KDATA	47	48	KEYBD - CLK
KEYBD - +5V	49	50	KEYBD - +5V

2.21 Jumper/Connector Summary

Connector/ Jumper	Description	Page Reference
J1	RS-422/RS-485 I/O Connector	2-7, 2-8, 2-9
J2	I/O Connector	2-19
J3	Floppy Disk I/O Connector	2-12
J4	IDE I/O Connector	2-12
J5	COM2 Configuration Jumper	2-5, 2-6, 2-7, 2-9
J6	COM1 Configuration Jumper	2-5, 2-6, 2-7, 2-8
J7	8255 Parallel I/O Connector	2-18
J8	CPU Speed Shift Enable Jumper	N/A
J9	Interrupt Routing Header	2-15
J10	Not Used	
J11	CPU Speed Select Jumper	2-2
J12	Processor Type Select	2-1
J13	NMI Routing Jumper	2-1
J14	Parallel I/O Vcc Routing Jumper	2-18
J15	Processor Type Select	2-1
J16	ECP DRQ Select Jumper	2-10
J17	Cache Control Jumper	2-1
J18	Processor Type Select	2-1
J19	Processor Type Select	2-1
J20	PC/104-8 Bus Connector	2-11
J21	PC/104-16 Bus Connector	2-11
J22	ECP DACK Select Jumper	2-10
J23	Watchdog Configuration Jumper	2-13
J24	SSD Array Size Select Jumper	2-17
J25	Power/Reset Connector	2-14
J26	Master Battery Enable Jumper	2-14
J27	SSD Write Protect Jumper	2-18
J28	SSD/DOC Mode Select Jumper	2-16
J29	U26 Battery Select Jumper	2-17
J30	U27 Battery Select Jumper	2-17
J31	U26 Device Configuration Jumper	2-17
J32	U27 Device Configuration Jumper	2-17
J33	Flash Write Enable Jumper	N/A

3 AWARD BIOS Configuration

3.1 General Information

The SAT-DX comes equipped with a standard Award BIOS with Setup in ROM that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM so that it retains Setup information when power is turned off.

3.2 Entering Setup

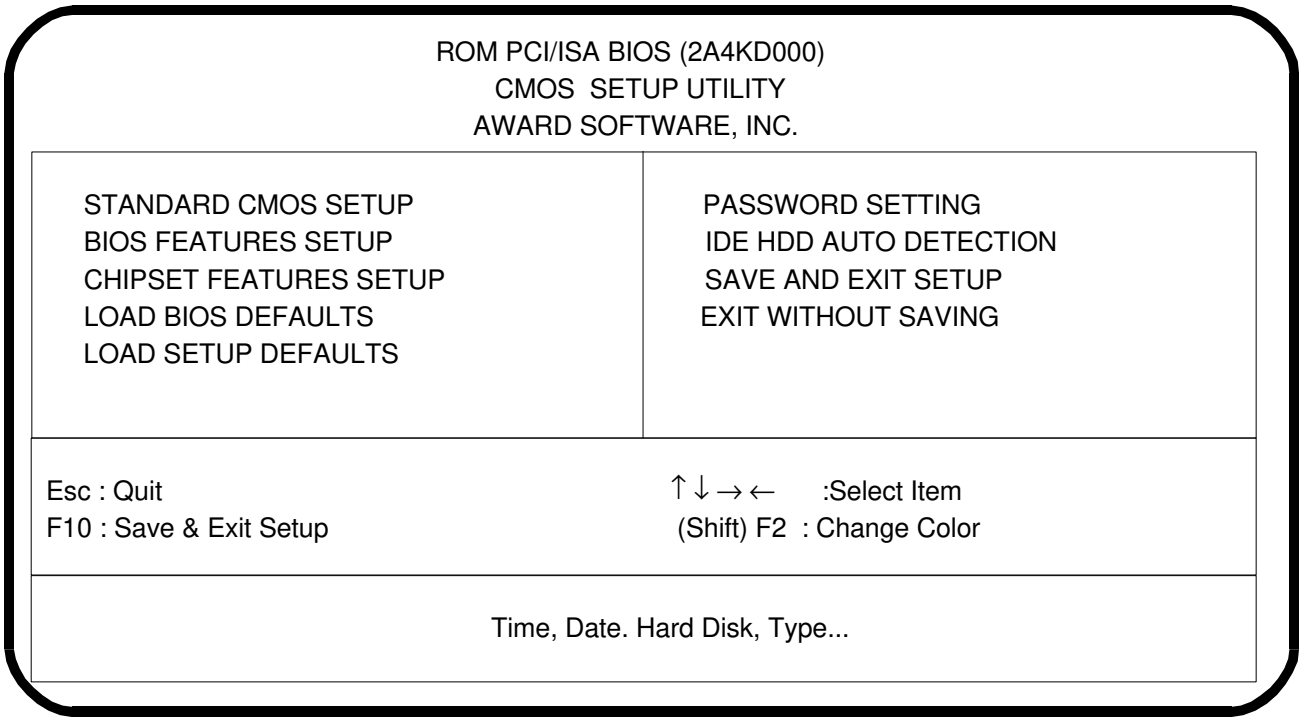
To enter setup, power on the computer and press the DEL key immediately after the message "Press DEL to Enter Setup" appears on the lower left of the screen. If the message disappears before you respond and you still wish to enter setup, restart the system by turning it OFF and then ON or by pressing the RESET button, if so equipped or by pressing the CTRL, ALT and DEL keys simultaneously. Alternately under certain error conditions of incorrect setup the message :

"Press F1 to continue or DEL to Enter Setup"

may appear. To Enter Setup at that time press the DEL key, to attempt to continue, ignoring the error condition, press the F1 key.

3.3 Setup Main Menu

The main menu screen is displayed on the following page. Each of the options will be discussed in this section. Use the arrow keys to highlight the desired selection and press ENTER to enter the sub-menu or to execute the function selected.



3.4 Standard CMOS Setup

The items in the Standard CMOS Setup menu are divided into several categories. Each category may include one or more setup items. Use the arrow keys to highlight the item and then use the PgUp, PgDn, + , -, keys to select the desired value for the item.

Date

The date format is <day>, <date>, <month>,<year>

day = The day, from Sun to Sat, determined by the BIOS and is display only.

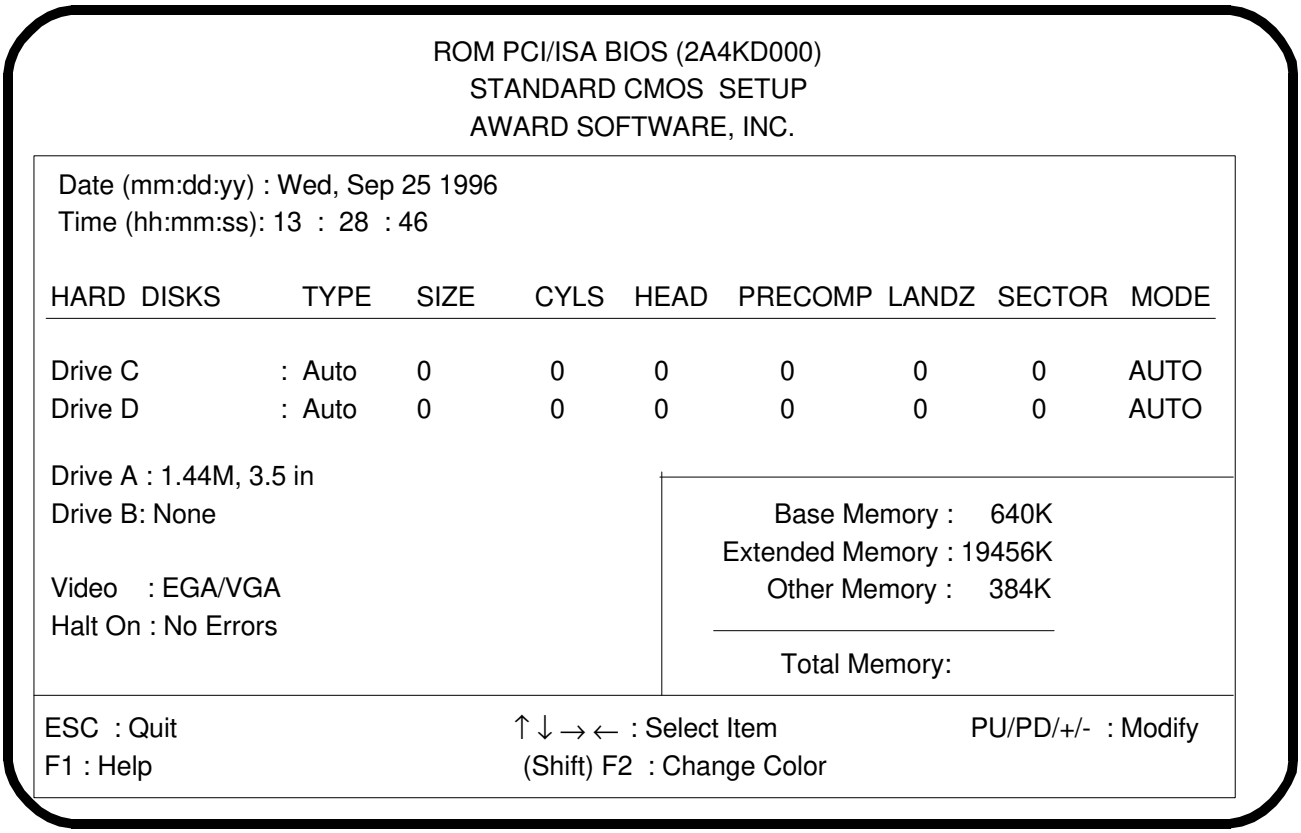
date = The date, from 1 to 31 (or the maximum for the current month)

month = The month, Jan through Dec

year = The year, from 1900 to 2099

Time

The time format is < hour> < minute> < second> . The time is calculated on the 24-hour military-time clock, such that 1:00PM is 13:00:00.



Drive C: type/Drive D: type

This category identifies the type of hard disk C: or hard disk D: that have been installed in the system. There are 46 predefined types and a user definable type. Types 1-46 are predefined as shown in the following table.

Type	Size	Cylinders	Heads	Sectors	Precomp	Landzone
1	10	306	4	17	128	305
2	20	615	4	17	300	615
3	30	615	6	17	300	614
4	62	940	8	17	512	940
5	46	940	6	17	512	940
6	20	615	4	17	None	615
7	30	462	8	17	256	511
8	30	733	5	17	None	733
9	112	900	15	17	None	901
10	20	820	3	17	None	820
11	35	855	5	17	None	855
12	49	855	7	17	None	855
13	20	306	8	17	128	319
14	42	733	7	17	None	733
15		Reserved				
16	20	612	4	17	0	663

17	40	977	5	17	300	977
18	56	977	7	17	None	977
19	59	1024	7	17	512	1023
20	30	733	5	17	300	732
21	42	733	7	17	300	732
22	30	306	5	17	300	733
23	10	977	4	17	0	336
24	40	1024	5	17	None	976
25	76	1224	9	17	None	1023
26	71	1224	7	17	None	1223
27	111	1224	11	17	None	1223
28	152	1024	15	17	None	1223
29	68	1024	8	17	None	1023
30	93	918	11	17	None	1023
31	83	925	11	17	None	1023
32	69	1024	9	17	None	926
33	85	1024	10	17	None	1023
34	102	1024	12	17	None	1023
35	110	1024	13	17	None	1023
36	119	1024	14	17	None	1023
37	17	1024	2	17	None	1023
38	136	1024	16	17	None	1023
39	114	918	15	17	None	1023
40	40	820	6	17	None	820
41	42	1024	5	17	None	1023
42	65	1024	5	26	None	1023
43	40	809	6	17	None	852
44	61	809	6	26	None	852
45	100	776	8	33	None	775
46	203	684	16	38	None	685

Press <PgUp> or <PgDn> to select a numbered hard disk type, or type the number and press Enter. Most manufacturers supply hard disk information with their drives than can be used to help identify the proper drive type. Modern IDE drives seldom fall into the predefined types and are usually best handled with the “auto” or “user” defined types. The “auto” mode, reads the hard disk type information at boot time and uses it. The “user” mode allows for either manual or automatic entry, via the setup option “IDE Auto Detect” of the drive parameters.

If you decide to create the user type manually you must supply the required parameters as to Cylinder count, Head count, Precomp Cylinder, Landing Zone Cylinder, and number of sectors per track.

On fixed disks larger than 528MB it will also be necessary to choose the Logical Block Addressing (LBA) mode if you wish the drive to be accessible as a single drive letter.

If there is no hard disk installed be sure to select type “none”.

Drive A: type/Drive B: type

This category identifies the type of floppy drives attached as Drive A: or Drive B:. The choices are as follows :

NONE
360K, 5.25 in.
1.2M, 5.25 in.
720K, 3.5 in.
1.44M, 3.5 in.
2.88M, 3.5 in.

Note that the standard SAT-DX board does not support the 2.88M floppy drives. If 2.88M floppy support is required, contact your WinSystems' Applications Engineer to inquire about this option.

VIDEO

This category specifies the type of video adapter used for the primary system monitor that matches your video display board and monitor. The available choices are :

EGA/VGA
CGA40
CGA80
MONO

It is recommended that if no display card is present that EGA/VGA be chosen.

Error Halt

This category determines whether the system will halt if a nonfatal error is detected during the power up self test. The choices are :

No Errors : The system will not be stopped for any error that may be detected.

All Errors : Whenever the BIOS detects a nonfatal error the system will be stopped and a prompt will appear.

All, but Keyboard : The system will not stop for a keyboard error, it will stop for all other errors.

All but Diskette : The system will only stop on Disk errors. All other will be ignored.

All but Disk/Key : All errors except disk and keyboard will result in a halt and a prompt.

Memory

This category is display only and is determined by the BIOS POST (Power On Self Test).

Base Memory

The post routines in the BIOS will determine the amount of base (or conventional) memory installed in the system. The value of the base memory is typically 640K for systems with a Megabyte or greater of RAM installed.

Extended Memory

The BIOS determines how much extended memory is present during the POST. This is the amount of memory located above 1MB in the CPU's memory address space.

Other Memory

This refers to memory located in the 640K to 1024K address space. This is memory that can be used for different applications. DOS may use this area to load device drivers and TSRs to keep as much base memory free as possible for application programs. The most common use of this area is for Shadow RAM.

3.5 BIOS Features Setup

Virus Warning

This option when enabled, protects the boot sector and partition table of the hard disk against unauthorized write through the BIOS. Any attempt to alter these areas will result in an error message and a prompt to authorize the activity or not.

CPU Internal Cache

This option when enabled provides maximum performance by caching instructions and data using the on-chip cache of 486 processors.

Quick Power On Self Test

This option when enabled, speeds up the POST during power up. If it is enabled the BIOS will shorten and/or skip some test items during POST.

ROM PCI/ISA BIOS (2A4KD000)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.

Virus Warning	: Disabled	Video BIOS Shadow	: Enabled
CPU Internal Cache	: Enabled	C8000-CFFFF Shadow	: Disabled
		D0000-D7FFF Shadow	: Disabled
Quick Power On Self Test	: Enabled	D8000-DFFFF Shadow	: Disabled
Boot Sequence	: A,C		
Swap Floppy Drive	: Disabled		
Boot Up Floppy Seek	: Disabled		
Boot Up NumLock Status	: Off		
Boot Up System Speed	: High		
Gate AZO Option	: Fast		
Typematic Rate Setting	: Disabled		
Typematic Rate (Chars/Sec)	: 6	ESC : Quit	↑ ↓ → ← : Select Item
Typematic Delay (Msec)	: 250	F1 : Help	PU/PD/+/- : Modify
Security Option	: Setup	F5 : Old Value	Shift) F2 : Color
		F6 : Load BIOS Defaults	

Boot Sequence

This option determines the boot attempt sequence for the fixed disk and floppy disk. The choices are:

C,A System will attempt Hard disk boot first
A,C System will attempt Floppy disk boot first

Swap Floppy Drive

This option allows for swapping of the A: and B: floppy drives without actually relocating the drives on the cable.

Boot Up Floppy Seek

During POST, when this option is enabled, the BIOS will determine if the floppy drive is 40 tracks or 80 tracks. If disabled, no seek test will be performed and no error can be reported.

Boot Up Numlock Status

This allows user selection of the Numlock state at Boot time.

Boot Up System Speed

This option allows specification of the processor speed at boot time. The options are :

FAST
SLOW

Gate A20 Option

This option allows selection of the source for the gate A20 signal. The choices are :

Normal - Sourced from keyboard controller
Fast - Sourced from the Chipset

Typematic Rate Setting

This enables or disables typematic rate programming at boot time. Typematic is the auto-repeat function for the keyboard.

Typematic Rate

When the typematic rate setting is enabled the typematic repeat speed is set via this option. The supported rates are :

6 characters per second
8 characters per second
10 characters per second
12 characters per second
15 characters per second
20 characters per second
24 characters per second
30 characters per second

Typematic Delay

When typematic rate setting is enabled, this option specifies the time in milliseconds before auto-repeat begins. The supported values are :

250mS
500mS
750mS
1000mS

Security Option

This option allows you to limit access to the system and setup or just to setup. The choices are :

System - The system will not boot and access will be denied if the correct password is not entered at the prompt.

Setup - The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

NOTE : To disable security, select "Password Setting" at the Setup Main Menu and then you will be asked to enter a password. Do not type anything but just hit ENTER. Once the security is disabled, the system will boot and you can enter Setup freely.

Shadowing Options

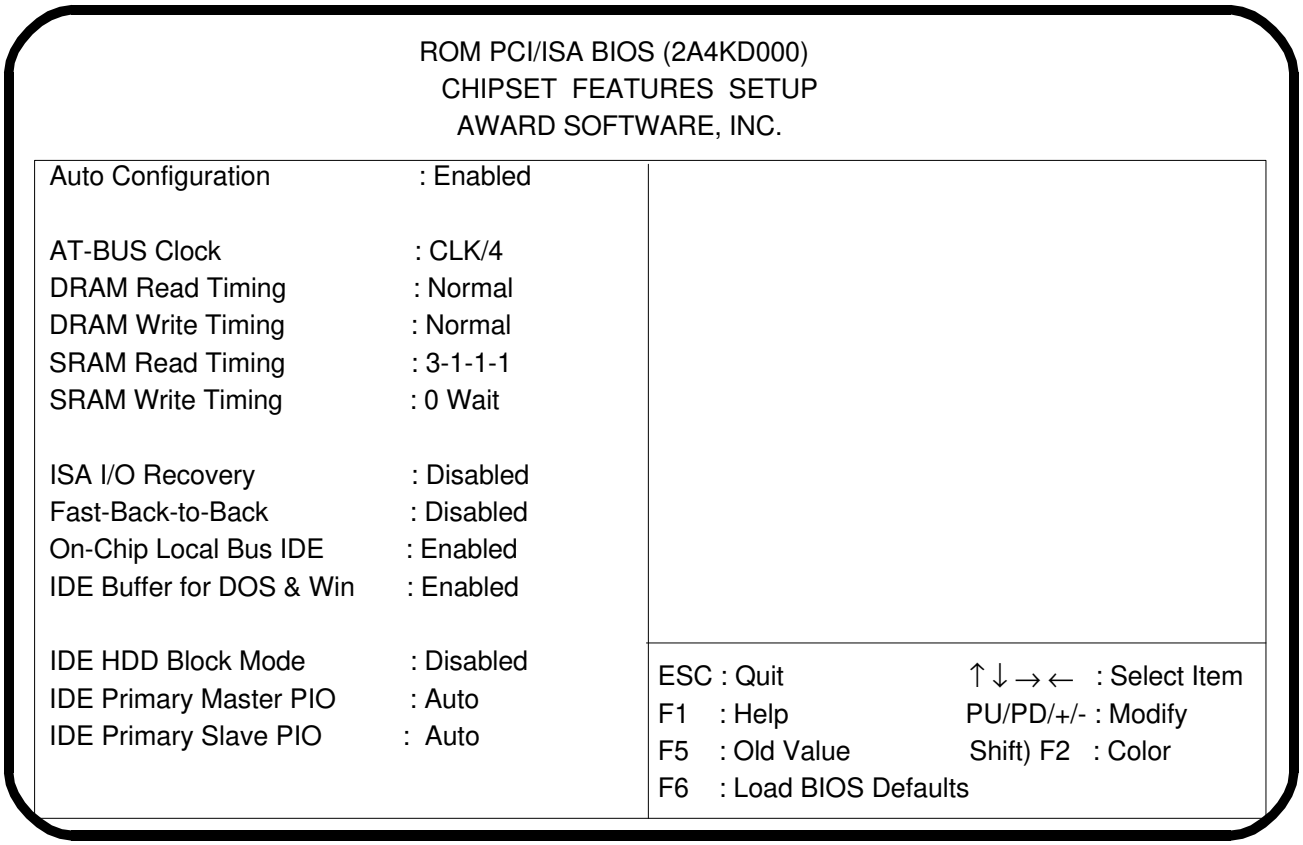
When shadowing for a particular address range is enabled, it instructs the BIOS to copy the BIOS located in ROM into DRAM. This shadowing from an 8-bit EPROM into fast 32-bit DRAM results in a multi-magnitude performance increase. The main BIOS is shadowed automatically but there are other areas that may be selected for shadowing. There areas available for shadowing are shown here :

Video BIOS Shadow - C000-C7FFF EGA/VGA BIOS ROM
C8000-CFFFF
D0000-D7FFF
D8000-DFFFF

3.6 Chipset Features Setup

The options in this section control the chipset programming at boot time. In most cases, the default settings should be used unless you have a clear understanding of the significance of the change. It is possible using these options to create a system that will either not boot at all or is very unstable or unreliable. If this should occur, there are two alternatives to return the system to a stable configuration. If the system works well enough to get into Setup, simple choose the "Load BIOS Defaults" option and then "Save and Exit Setup" to restore to factory defaults. If the system will not run well enough to run setup, it will be necessary to remove the battery source temporarily. Refer to section 2.6 for details on reinitializing the CMOS RAM.

Each of the options for the Chipset Features Menu will be briefly discussed in the pages that follow.



Auto Configuration

This option, when enabled, instructs the BIOS to auto- select the proper AT Bus Clock, the DRAM read timing, the DRAM write timing, the SRAM read timing, and the SRAM write timing based upon its determination of CPU speed. The default is “Enabled”.

AT Bus Clk

This option is available when the “Auto Configuration” option is disabled. This allows selection of the speed of the AT-BUS clock. This clock is any one of 5 sub-multiples of the processor oscillator or is a fixed 7.19Mhz. The Choices available are :

7.19Mhz
CLK/3
CLK/4
CLK/5
CLK/6
CLK/8

DRAM Read Timing

This option controls the read timing to the DRAM array. The available options are shown here :

slow
normal - default
fast
fastest

DRAM Write timing

This option control the write timing to the DRAM array. The available options are shown here :

slow
normal - default
fast
fastest

SRAM Read Timing

This option allows for the selection of timing patterns used to access the cache RAM. The available choice are :

2-1-1-1
3-1-1-1 Default
3-2-2-2
4-2-2-2

SRAM Write timing

This option controls the number of wait states to be inserted during cache write operations. The choices are :

0 Wait
1 Wait Default

ISA I/O Recovery

The CPU and local bus are much faster than the standard for the ISA bus. Selecting Enabled, allows additional time for I/O devices to respond to the system, otherwise data could be lost. The default setting is Enabled.

Fast Back-to-Back

When Enabled, consecutive write cycles targeted to the same slave become fast back-to-back on the PCI bus. The default setting is Disabled.

On-Chip Local BUS IDE

This option when enabled allows usage of the onboard local bus IDE controller. The default is Enabled.

IDE Buffer for Dos & Win

Select Enabled to increase throughput to and from IDE devices by using the on-chip read-ahead and post-write IDE buffers. Note that the use of the buffers may cause some slow IDE devices to appear even slower. The default is Enabled.

IDE HDD Block Mode

Block mode is also called block transfer, multiple command, or multiple sector read/write. If the IDE hard drive supports block mode, select Enabled for automatic detection of the optimal number of block reads/writes per sector that the drive can support. The default is disabled.

IDE Primary Master PIO

There are 5 transfer modes available for hard disk IDE transfers ranging from mode 0 to mode 4 with each successive mode providing an increased level of performance. Selecting Auto will allow the BIOS to automatically select the optimum transfer mode for the master hard disk. The default is Auto.

IDE Primary Slave PIO

Like the previous item, this option allows for the selection of any one of 5 IDE transfer modes or an Auto selection which allows the BIOS to auto-optimize the IDE transfers to/from the slave drive. The default is Auto.

3.7 Load BIOS Defaults

This main-menu option will cause the CMOS to be loaded with the default values assigned by the factory. These are usually considered safe values and do not necessarily represent the highest performance values.

3.8 Load Setup Defaults

The options will cause the CMOS to be loaded with the default Setup values assigned by the factory. These are usually values that were determined to give a higher level of performance along with reliable operation.

3.9 Password Setting

This option allows the setting of the security password. Pressing Enter at the password prompt disables the security function completely.

3.10 IDE HDD Auto Detection

This function allows modern IDE fixed disks to be used to their maximum potential by interrogating the drive as to its preferred configuration of tracks, heads, and sectors and automatically loading these parameters into a “user defined” hard disk type.

3.11 Save & Exit Setup

This function writes all changes to CMOS RAM and restarts the system.

3.12 Exit without Saving

This option exits Setup without saving any changes made and then restarts the system.

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4 SAT-DX Silicon Disk Reference

4.1 Introduction

WinSystems provides silicon disk support for the SAT-DX using four different media types depending upon the needs of the application.

1. The SAT-DX provides support for a bootable ROMDISK with a size of up to 1.44 Megabytes. A simple disk imaging technique allows for the easy creation and maintenance of ROMDISKS. Since the bootable ROMDISK is an exact image of a bootable floppy diskette, all testing and debugging can be accomplished using a floppy drive. Once the application is ready for ROM, it's a simple matter to use the MKDISK utility to create the EPROM files necessary for the bootable ROMDISK equivalent of the functioning floppy diskette.

2. In applications requiring occasional program or data updates PEROM (Flash) disks of up to 1 Megabyte may be used as the boot media. Onboard support is provided for the formatting, reading, and writing of the Floppy drive emulating PEROMS.

3. For Applications needing to log data, update the application, or for convenience during development, battery backed SRAM may be used as the boot media with a size of up to 1 Megabyte.

4. The SAT-DX supports the M-Systems' Disk-On-Chip Devices (DOC). These are single chip devices containing the BIOS Extension, TFFS Flash File System, and a Flash array ranging in size from 2 Megabyte to 72Megabytes. These devices emulate a Hard disk at the BIOS level.

4.2 ROMDISK Usage

MKDISK is a menu driven utility for creating the ROM image(s) duplicating the desired floppy diskette. MKDISK is invoked at the DOS command line with :

MKDISK

Select the USSD mode from menu number 1. The other menu options are used with other WinSystems' Silicon Disk systems and are NOT compatible with the SAT-DX board.

MKDISK - Solid State RomDisk Creation Utility V6.00
(C) 1988-1994, WinSystems Inc.

SELECT SSD TYPE

Paged Memory Mode (SSD-XT)
Extended Memory Mode (SSD-AT)
V53 Expanded Memory Mode
I/O Mapped Silicon Disk (USSD)
sx386 On Board ROMDISK
SBC53sx Expanded Memeory Mode
SAT-V40 Expanded Memory Mode

Use arrow keys and ENTER to make your selection.

MKDISK - Main Menu

From menu number 2 select the appropriate source disk size and type.

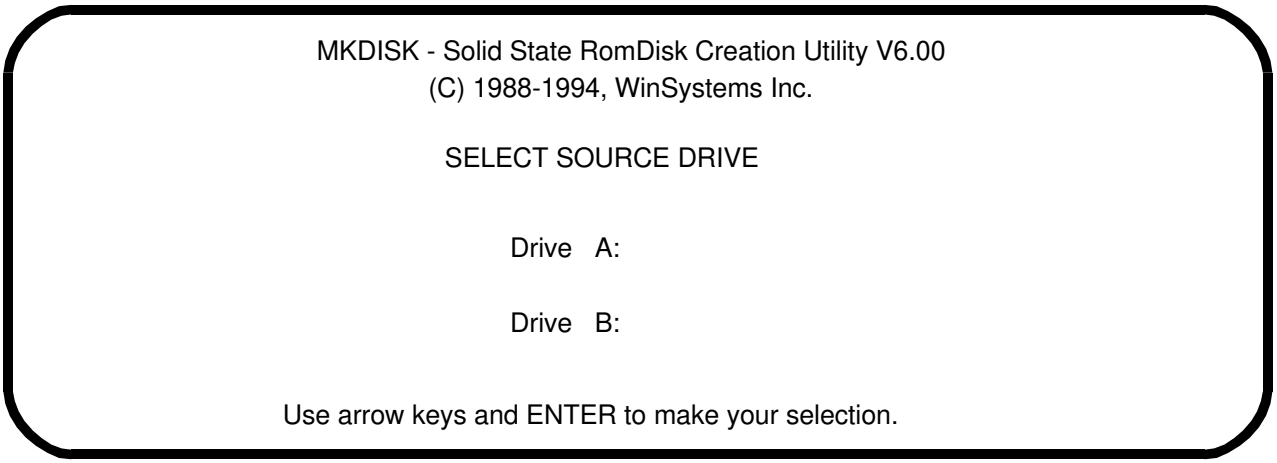
MKDISK - Solid State RomDisk Creation Utility V6.00
(C) 1988-1994, WinSystems Inc.

SELECT SOURCE DISK TYPE

160 KB 5 1/4 Single Sided 8 Sectors 40 tracks
180 KB 5 1/4 Single Sided 9 Sectors 40 tracks
320 KB 5 1/4 Double Sided 8 Sectors 40 tracks
360 KB 5 1/4 Double Sided 9 Sectors 40 tracks
720 KB 3 1/2 Double Sided 9 Sectors 80 tracks
720 KB 5 1/4 Double Sided 9 Sectors 80 tracks
954 KB 3 1/2 Double Sided 9 Sectors 53 tracks
960 KB 5 1/4 Double Sided 15 Sectors 64 tracks
1.2 Meg 5 1/4 Double Sided 15 Sectors 80 tracks
1.4 Meg 3 1/2 Double Sided 18 Sectors 80 tracks

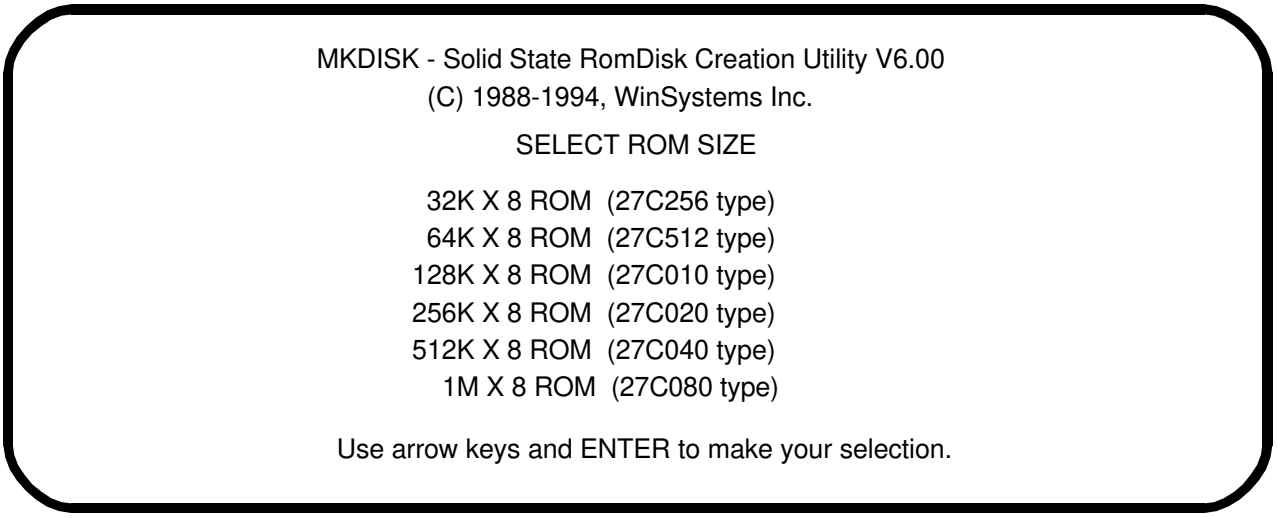
Use arrow keys and ENTER to make your selection.

MKDISK - Drive type Menu



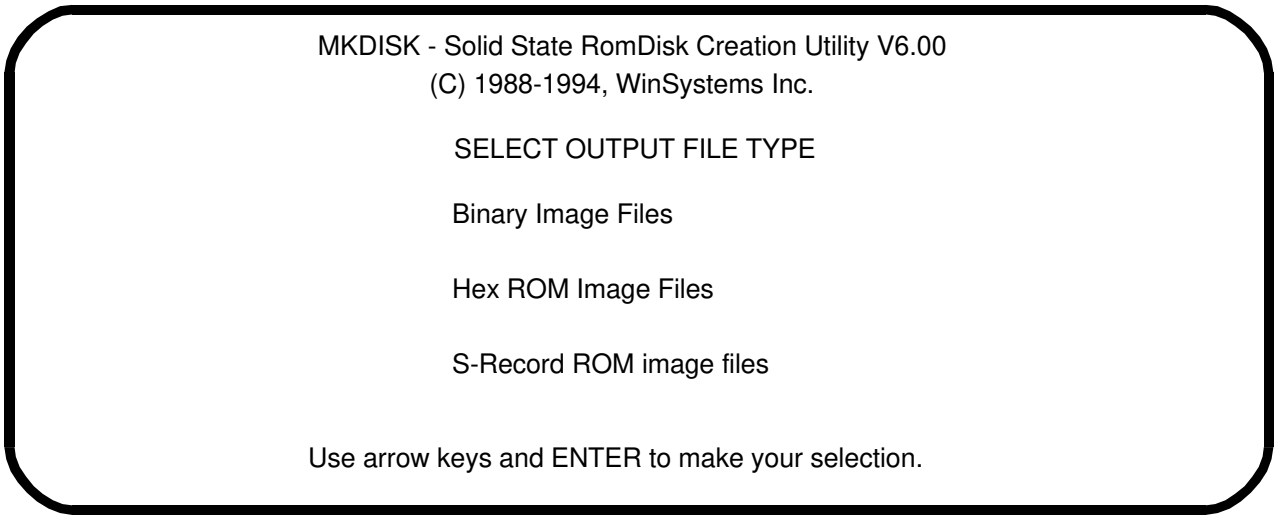
MKDISK - Drive Menu

Select the source drive as appropriate.



MKDISK - ROM type Menu

From menu number 4 select the appropriate EPROM size for the ROMDISK. EPROM sizes smaller than 512K or not usable with the SAT-DX, but are provided as choices with other silicon disk devices.



MKDISK - Output Menu

From menu number 5 select the appropriate ROM image file format that your EPROM programmer accepts. Selecting the Binary ROM image file format will result in the smallest files. MKDISK will then read the specified floppy diskette and create a ROMx.HEX or ROMx.S19 where x is the ROM number in the sequence (starting with 1) and the extension (.BIN, .HEX, .S19) indicates the output format for Binary, Hex, and Motorola respectively. If more than one file is created it means that the disk will span more than a single EPROM. Once the ROM(s) have been created using the image files, install the ROM(s), jumper for correct ROM size, and enable the Silicon Disk boot option. The next power up should result in a boot from the A: Silicon Disk. The actual floppy drive, if present, will then be available as drive B:.

4.3 Bootable RAMDISK usage

The SAT-DX supports bootable RAMDISKs of up to 1 Megabyte in size. 512K X 8 Static RAMs/PEROMs can be installed in the board beginning at U27. One or two RAMs/PEROMs can be installed and the device jumpers should be appropriately set as described in section 2.20. After powerup it is necessary to configure the silicon disk for the actual size of the drive using the SSDINIT utility. SSDINIT is invoked at the DOS command line with :

```
SSDINIT [A: | B: ] disk_size[K | M]
```

the K or M arguments are optional and are actually ignored. Values below 32 are assumed to be in Megabytes while values above 32 are assumed to be in Kilobytes. An example might help to clarify. To prepare a 1meg FLASH or SRAM disk for formatting type :

```
SSDINIT B: 1M
```

The disk is new and prepared for formatting. The system must be rebooted prior to formatting with the simple DOS command :

```
format b: /s/u
```

After the next reset the formatted silicon disk will boot as the A: drive. If it is ever necessary to bypass the silicon disk boot in order to reformat or to boot the actual floppy drive, or the hard disk, simply press the < CTRL> < ALT> < LSHIFT> keys simultaneously immediately following display of the BIOS configuration BOX. The message :

```
Silicon Disk Boot Aborted by User
```

will be displayed and the system will boot from one of the available boot drives.

IMPORTANT NOTE : The FLASHDISK is fully writeable at all times but is not recommended for continuous updating or data logging. The onboard BIOS implements a simple FAT based file system (identical to a floppy disk) with no wear leveling implemented. The PEROMS can and will wear out with excessive write cycles. ATMEL specifies at least 10,000 write cycles.

4.4 Non-Bootable RAMDISK Usage

A non-bootable RAMDISK is often desired in conjunction with a bootable ROMDISK, FLASHDISK, or rotational media. It can then be used for program updates, parameter storage, or data logging applications. a non-bootable RAMDISK uses the WinSystems' Universal Solid State Disk Driver (USSD) which is loaded via the boot media's CONFIG.SYS file with the entry :

```
device = ussd.sys /mod:p /pad:1d4 /seg:e400 /psz:16 /inc:1 /spg:xx /dsz:yy
```

where the YYY in /DSZ:YYY is the size of the disk in Kilobytes and the XXX in the /SPG:XXX is the starting page address in the array for this silicon disk. This hexadecimal value is actually the count of 16K byte blocks preceding the start of the RAMDISK. The simplest approach is to use the table below to determine the correct /SPG value.

Total RAM/ROM/FLASH Prior to this socket	/SPG Value
None	/SPG:80
512K	/SPG:A0
1M	/SPG:C0

A couple of examples might help to illustrate. Suppose we're booting from a floppy or hard disk and we have installed two 512K X 8 SRAMs. In order to create the desired 1 Meg RAMDISK we would need the line :

```
device = ussd.sys /mod:p /seg:e400 /psz:16 /inc:1 /pad:1d4 /spg:80 /dsz:1024
```

which would indicate that we wish to create a disk of 1M (1024K) starting at the beginning of the array.

For another example assume that we want a 512K ROMDISK and a 512K RAMDISK. We would create our bootable floppy with the CONFIG.SYS line :

```
device = ussd.sys /mod:p /pad:1d4 /seg:e400 /psz:16 /inc:1 /spg:a0 /dsz:512
```

which would create the 512K RAMDISK which will be preceded by the 512K of ROMDISK. We would create our ROMDISK as previously described and place the EPROM into U27. We would install our 512K SRAM into U26.

A final example would be to use the non-bootable RAMDISK in U26 as a secondary silicon disk to a DISK-ON-CHIP. In this case we are booting from the DISK-ON-CHIP and will include the following CONFIG.SYS command line :

```
device =  ussd.sys /mod:p /seg:e400 /psz:16 /inc:1 /pad:1d4 /spg:A0 /dsz:512
```

This will create a 512K RAMDISK in the silicon disk socket U27.

NOTE : USSD, as is the convention with DOS installable disk devices, creates a drive with the NEXT AVAILABLE drive letter. Drives A: and B: are always reserved for the physical floppy drive or the BIOS supported bootable Silicon Disk. In a system without a hard disk, the next available drive letter would be C:. In a system with one or more hard drive partitions, the silicon disk created with USSD will be the first available letter following any other drive letters already in use. Also note that it is never necessary to format a disk created with USSD. The disks are self formatting using the size and address information provided on the CONFIG.SYS invocation line. During initialization, USSD examines the silicon disk to determine if a disk already exists which matches the parameters specified. If so, no action is taken and the disk is used as is. If there is not a disk of the type and size specified, it is created.

4.5 Non-Bootable Flash Disk Usage

The ATMEL 5 Volt Flash Parts (29C040/29C040A) may also be used as a non-bootable drive in a manner nearly identical to the RAMDISK usage described in the previous section. The only change when using USSD for the ATMEL PEROMs is the addition of the

/EPT:256 parameter to the CONFIG.SYS line which installs the USSD driver. An example using a 512K EPROM for a ROMDISK and a 512K PEROM device would need the line :

```
device = ussd.sys /mod:p /pad:1d4 /seg:e400 /psz:16 /inc:1 /spg:a0 /dsz:512 /ept:256
```

in the CONFIG.SYS file on the floppy to be image. This invocation will create a 512K Flash disk in the second socket of the array. Refer to the previous section on non-bootable RAMDISK usage for additional details regarding the USSD driver.

4.6 DiskOnChip Usage

The SAT-DX supports the M-Systems' Disk-On-Chip (DOC) Flash device in sizes ranging from 2MB to 72MB. The DOC device contains a BIOS extension, the TFFS (Tiny Flash File System), and the flash memory all in a single 32-pin device. The DOC unlike the other WinSystems' SSD support for the SAT-DX emulates a hard disk rather than a floppy disk. The DOC can be used as a secondary hard disk to a physical IDE drive or it can be the only hard disk in the system.

The DOC is installed into the socket at U27. Refer to section 2.18 for correct device jumpering and enabling of the DOC.

4.6.1 DOC Initialization

The DOC is initialized in an identical fashion to a fixed disk. DOS is booted (from floppy or hard disk), FDISK is run on the DOC drive (Be sure to get the right drive), the system is rebooted and then the DOC is formatted using the DOS format command.

If the /S switch was used during formatting and there is no other fixed disk device specified or attached to the systems the DOC will become the boot device. If a hard disk is present the DOC will become a secondary fixed disk.

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5 APPENDIX A

I/O Port Map

The following is a list of PC I/O ports. Addresses marked with a '-' are not used on the SAT-DX but their use should be carefully qualified so as not to conflict with other I/O boards. I/O addresses marked with a '+ ' are used by the SAT-DX board and are unique to the WinSystems' design. I/O Addresses marked with '**' are generally unused and should be the basis for the first choices in I/O address selection.

Hex Range	Usage
000-00F	8237 DMA #1
**0010-01F	FREE
020-021	8259 PIC #1
+022-023	FINALI Chipset Registers
**024-03F	FREE
040-043	8254 Timer
**04405F	FREE
060-06F	8042 Keyboard controller
070-071	CMOS RAM/RTC
*0072-07F	FREE
080-08F	DMA Page Registers
**090-09F	FREE
0A0-0BF	8259 PIC #2
0C0-0DF	8237 DMA #2
**0E0-0FF	FREE
0F0-0F1	Coprocessor Control
0F2-1CF	FREE
+1D0-1DF	Watchdog timer, SSD Control and SSD configuration
**1E0-1EF	FREE
1F0-1FF	Fixed Disk I/O
-200-20F	Joystick Port
-210-21F	PCM-SSD I/O Ports
-220-22F	Soundblaster I/O Ports
**230-237	FREE
-238-23B	BUS Mouse
**240-277	FREE
278-27F	LPT1
**280-2AF	FREE
-2B0-2DF	EGA Video
-2E0-2E7	GPIB Interface
-2E8-2EF	COM4
**2F0-2F7	FREE
2F8-2FF	COM2
-300-31F	Prototype Card
-320-32F	XT Hard Disk
**330-377	FREE

-378-37F	Parallel Printer
-380-3AF	SDLC
-3B0-3BB	MDA
-3C0-3CF	EGA Video
-3D0-3DF	CGA
**3E0-3E7	FREE
-3E8-3EF	COM3
3F0-3F6	Floppy Disk
3F8-3FF	COM1

6 APPENDIX B

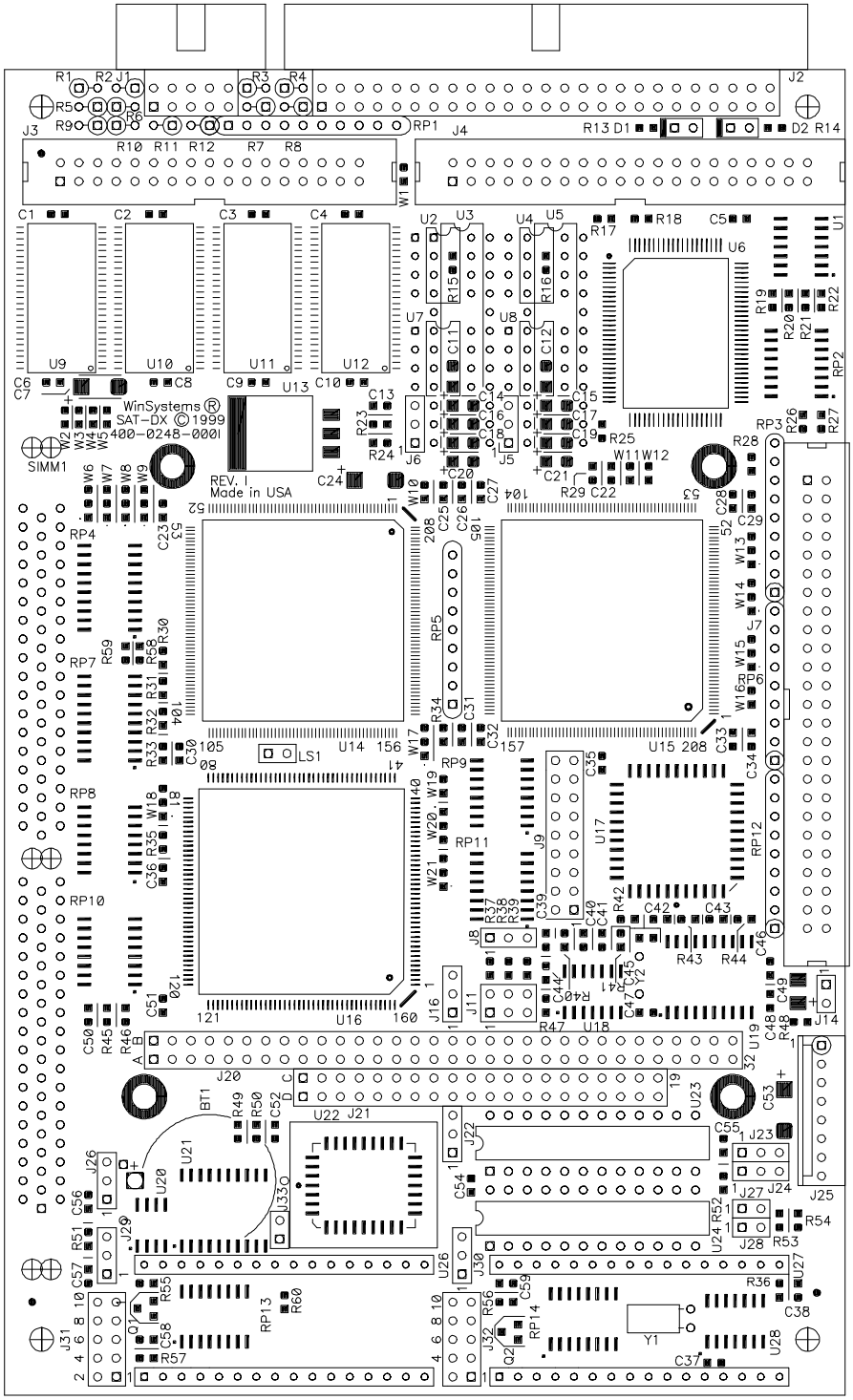
Interrupt Map

No.	Address	Type	Description
0	00	CPU	Divide by 0
1	04	CPU	Single Step
			386 Debug Exception
2	08	CPU	MI
3	0C	CPU	Breakpoint
4	10	CPU	Overflow
5	14	BIOS	Print Screen
		186	Bound Fault Exception
6	18	186	Invalid Opcode Exception
7	1C	186	Coprocessor unavailable
8	20	Hardware	IRQ0 - 18.2 Hz heart beat
		286	LIDT - Double fault exception
9	24	Hardware	IRQ1- Keyboard interrupt
		286	Coprocessor Segment
A	28	Hardware	IRQ2 - XT Reserved, AT - Slaved Controller
		286	Invalid TSS exception
B	2C	Hardware	IRQ3 - COMM2
		286	Segment not present
C	30	Hardware	IRQ4 - COMM1
		286	Stack fault exception
D	34	Hardware	IRQ5 - XT Hard Disk, AT = LPT
		286	Protection fault exception
E	38	Hardware	IRQ6 - Floppy Disk Interrupt
		386	Page fault exception
F	3C	Hardware	IRQ7 - LPT1
10	40	BIOS	Video BIOS functions
		286	Coprocessor error exception
11	44	BIOS	BIOS Equipment check
		486	Alignment check exception
12	48	BIOS	Memory size function
13	4C	BIOS	BIOS Disk functions
14	50	BIOS	BIOS Serial functions
15	54	BIOS	Cassette/Protected mode functions
16	58	BIOS	Keyboard BIOS functions
17	5C	BIOS	BIOS Printer functions
18	60	BIOS	SROM Basic Entry Point (IBM Only)
19	64	BIOS	Boot loader function
1A	68	BIOS	BIOS Time of Day functions
1B	6C	BIOS	Keyboard break vector
1C	70	BIOS	User chained timer tick
1D	74	BIOS	Video Initialization
1E	78	BIOS	Floppy Disk parameter table
1F	7C	BIOS	CGA graphic character font
20	80	MS-DOS	Program terminate

21	84	MS-DOS	DOS function call
22	88	MS-DOS	Terminate Address
23	8C	MS-DOS	Ctrl-Break exit address
24	90	MS-DOS	Fatal Error Vector
25	94	MS-DOS	Absolute disk read
26	98	MS-DOS	Absolute disk write
27	9C	MS-DOS	Terminate
28	A0	MS-DOS	Idle signal
29	A4	MS-DOS	TTY output
2A	A8	MS-DOS	MS-NET services
2F	BC	MS-DOS	Print Spool
30	C0	MS-DOS	Long jump interface
33	CC	MS-DOS	Mouse functions
3F	FC	MS-DOS	Overlay interrupt
40	100	BIOS	Floppy I/O when fixed disk present
41	104	BIOS	Hard disk 1 parameter table
42	108	BIOS	EGA Chain
43	10C	BIOS	EGA Parameter table pointer
44	110	BIOS	EGA graphics character font
4A	128	BIOS	AT Alarm exit address
50	140	BIOS	AT Alarm interrupt
51	144	BIOS	Mouse functions
5A	168	NET	Functions
5B	16C	NET	Boot chain
5C	170	NET	Net BIOS Entry
67	19C	MS-DOS	EMS Functions
6D	1B4	VGA	VGA Service
70	1C0	Hardware	IRQ8 - Real time clock
71	1C4	Hardware	IRQ9 - Redirected IRQ2
72	1C8	Hardware	IRQ10 - Unassigned
73	1CC	Hardware	IRQ11 - Unassigned
74	1D0	Hardware	IRQ12 - Unassigned
75	1D4	Hardware	IRQ13 - 80287 Coprocessor
76	1D8	Hardware	IRQ14 - AT Hard Disk
77	1DC	Hardware	IRQ15 - Unassigned
80	200		
F0	3C0	Basic	
F1	3C4		
FF	3FC	Not used	

7 APPENDIX C

SAT-DX Parts Placement Guide



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8 APPENDIX D

SAT-DX Parts List

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BEGINNING RANGE: SAT-DX2-66-0M ENDING RANGE: SAT-DX2-66-0M

LEVEL	ITEM KEY	ITEM DESCRIPTION	BOM DESCRIPTION	LOC	OVHD KEY	ITEM TYPE	QTY REQUIRED
1	SAT-DX2-66-0M	486 DX2 SBC, 66 MHZ, OMB SIMM DRAM					1
2	999-9999-001	SPECIAL NOTES	10-21-96 MEB (NEW)	ARLIN		Inv	1
2	0248-100-0000E	ASSY SAT-DX2-66-0M SIMM REV.E		ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	11-24-97 MEB 97-113	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	04-04-97 MEB ECO 97-28	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	10-21-96 MEB (NEW)	ARLIN		Inv	1
3	>603-1047-803	CAP .1uF 50v 20% CER 0805	C1-C8,C13,C18,C20,C22,C23,C25,C29-C31,	ARLIN		Inv	30
3	>999-9999-001	SPECIAL NOTES	C33,C34,C36,C39,C41,C42,C45,C47-C52	ARLIN		Inv	1
3	>603-1037-803	CAP .01uF 50v 20% CER 0805	C32,C35,C43,C44,C53	ARLIN		Inv	5
3	>603-2207-403	CAP 22pF 50v 1% NPO 0805	C24,C28,C37,C40	ARLIN		Inv	4
3	>603-1027-703	CAP 1000pF 50v 10% CER 0805	C38	ARLIN		Inv	1
3	>603-2255-82B	CAP 2.2uF 25v 20% TAN 3528	C26	ARLIN		Inv	1
3	>603-1065-82D	CAP 10uF 25v 20% TAN 6032	C27,C46	ARLIN		Inv	2
3	>603-1053-82A	CAP 1uF 16v 20% TAN 3216	C9-C12,C14-C17,C19,C21	ARLIN		Inv	10
3	>124-0017-000	LED GREEN RECTANGLE L-153GDT (KN	D1	ARLIN		Inv	1
3	>124-0016-000	LED RED RECTANGLE L-153HDT (KNGB	D2	ARLIN		Inv	1
3	>201-0010-121	HDR 2X5 RA PRO IDH-10LP-SR3-TR/T	J1	ARLIN		Inv	1
3	>601-0000-503	RES 0 Ohm 5% 1/10w 0805	J12B,J13,J15B,J18B,J19B,R100,R109,	ARLIN		Inv	11
3	>999-9999-001	SPECIAL NOTES	R119,R121,R122,R123	ARLIN		Inv	1
3	>201-0050-121	HEADER RA 2X25 IDH50LP-SR3-TR/TG	J2	ARLIN		Inv	1
3	>201-0034-021	HDR 34 POS ST IDH-34LP-S3-TG/TR	J3	ARLIN		Inv	1
3	>201-0040-021	HDR 40 PIN ST IDH-40LP-S3-TG/TR	J4	ARLIN		Inv	1
3	>201-0050-021	HDR 2X25 ST PRO IDH50LP-S3-TG/TR	J7	ARLIN		Inv	1
3	>201-0036-010	HDR 1X36 UN TSW-136-07-G-S (SAM)	J5,J6,J8,J16,J22-J24,J26,J29,J30=1X3	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J14,J28,J27=1X2	ARLIN		Inv	1
3	>201-0072-120	HDR 2X36 UN TSW-136-07-G-D	J9=2X9 J11=2X3 J31,J32=2X5	ARLIN		Inv	.62
3	>200-0064-000	SOCKET 64 POS QPHF2-64-020-1W (P	J20	ARLIN		Inv	1
3	>200-0040-000	SOCKET 40 POS QPFH2-40-020-1W (P	J21	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	INSTALL AFTER TEST, J26=1-2 (BATTERY)	ARLIN		Inv	1
3	>201-0008-601	HDR 8 POS MOLEX 22-11-2082	J25	ARLIN		Inv	1
3	>665-0001-102	TRANSISTOR 2N7002 (SOT-23)	Q1,Q2	ARLIN		Inv	2
3	>117-0102-050	RN SIP 10P-9 RES 1K L101S102 (BK	RP1	ARLIN		Inv	1
3	>121-0472-050	RN SIP 9P-8 RES 4.7KOh L09-1S472	RP2,RP3,RP5,RP8	ARLIN		Inv	4
3	>602-0103-512	RN 10K Oh, 5%, 2506/16 pin, Bus	RP4,RP7,RP9,RP10,RP11,RP12	ARLIN		Inv	6
3	>602-0102-512	RN 1K Ohm, 16 PIN, 15 RES BUSSED	RP6	ARLIN		Inv	1
3	>601-0103-503	RES 10K Ohm 5% 1/10W 0805	R20,R22,R24,R25,R27,R28,R33,R34,R96,R98	ARLIN		Inv	15
3	>999-9999-001	SPECIAL NOTES	R99,R106,R111,R113,R120	ARLIN		Inv	1
3	>601-0102-503	RES 1K Ohm 5% 1/10W 0805	R13,R14,R26,R29,R93,R94,R112,R114,R115,	ARLIN		Inv	11
3	>999-9999-001	SPECIAL NOTES	R117,R127	ARLIN		Inv	1
3	>601-0220-503	RES 22 Ohm 5% 1/10w 0805	R71,R74-R92,R101,R102,R124,R128	ARLIN		Inv	24
3	>601-2150-303	RES 215 Ohm 1% 1/10W 100V 0805	R95	ARLIN		Inv	1
3	>601-1210-303	RES 121 Ohm 1% 1/10w 0805	R97	ARLIN		Inv	1
3	>601-0331-503	RES 330 Oh, 5%, 0805	R103-R105,R108,R110	ARLIN		Inv	5
3	>601-0106-503	RES 10 MegOhm 5% 1/10w 0805	R107	ARLIN		Inv	1
3	>601-0101-503	RES 100 Ohm 5% 1/10w 0805	R116	ARLIN		Inv	1
3	>200-0072-120	SOCKET 72 PIN SIMM, RHT ANGL AMP	SIM1-HAND SOLDER, INSTALL BACK OF BOARD	ARLIN		Inv	1
3	>611-0004-001	IC, 74HC04M	U1	ARLIN		Inv	1
3	>250-0320-200	SKT STRP 32 POS SS-132-G-2 (SAM)	U2,U3,U4,U5,U7,U8	ARLIN		Inv	2.5
3	>200-0243-100	SOCKET 24 P .3 ICO-243-S8A-T (14	U21,U25	ARLIN		Inv	2
3	>621-0014-016	IC, I/O CNTRLR ALi M5113 1F2S1P	U6	ARLIN		Inv	1
3	>623-0006-016	IC, M1489 (24)	U14	ARLIN		Inv	1
3	>801-0101-200	IC, CS82C55A (25) HARRIS	U15	ARLIN		Inv	1

LEVEL	ITEM KEY	ITEM DESCRIPTION	BOM DESCRIPTION	LOC	OVHD KEY	ITEM TYPE	QTY REQUIRED
3	>670-0001-025	REGULATOR 5V-3.3V LINEAR TECH. L	U16	ARLIN		Inv	1
3	>622-0006-002	FREQ SYNTH 2-100MhZ AV9155-01CW2	U17	ARLIN		Inv	1
3	>620-0006-016	IC, 486 DX4-75 8K WB	U18	ARLIN		Inv	1
3	>623-0005-016	IC, M1487 (24)	U19	ARLIN		Inv	1
3	>650-0032-002	SOCKET 32P AMP 822273-1 (28)	U22	ARLIN		Inv	1
3	>622-0007-001	IC, MAX692ACSA (Maxim only!)	U23	ARLIN		Inv	1
3	>611-0273-002	IC, 74HC273M	U24	ARLIN		Inv	1
3	>250-0320-200	SKT STRP 32 POS SS-132-G-2 (SAM)	U26,U27	ARLIN		Inv	2
3	>220-0019-000	XTAL 14.31818 U49-20-143	Y1 - USE FOAM TAPE UNDER Y1	ARLIN		Inv	1
3	>220-0001-000	XTAL 32.768KHZ TF U3X832768	Y2 - USE FOAM TAPE UNDER Y2	ARLIN		Inv	1
3	>400-0248-000E	PCB, SAT-DX REV.E	*MASK:R1-R12	ARLIN		Inv	1
2	0248-300-0000E	SUB ASSY SAT-DX2-66 (75 MHZ CPU)		ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	05-26-98 MEB ECO 98-54	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	11-24-97 MEB ECO 97-113	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	11-24-97 MEB ECO 97-111	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	10-20-97 MEB ECO 97-99	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	09-02-97 MEB ECO 97-83	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	06-18-97 MEB ECO 97-43	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	06-03-97 MEB ECO 97-37	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	01-28-97 MEB ECO 97-06	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	10-21-96 MEB (NEW)	ARLIN		Inv	1
3	>111-0001-000	BAT 3V LI COIN CR2032-H04 (SONY)	BT1 - MUST BE HAND SOLDERED,	ARLIN		Inv	1
3	>730-0026-000	PIEZO TRANSDUCER BRP2407L-30	LS1 - MUST BE HAND SOLDERED	ARLIN		Inv	1
3	>111-0032-000	INSULATOR BATTERY CR2032	INSTALL UNDER BT1,LS1	ARLIN		Inv	2
3	>730-0083-000	IC, SP208CP (SIPEX), MAX208CNG (	U3,U5	ARLIN		Inv	2
3	>901-0011-000	IC, PALC22V10-35PC (15,TI) (17,C	U25 CS=5805 \SATDX\U25.JED	ARLIN		Inv	2
3	>999-9999-001	SPECIAL NOTES	U21 CS=E720 \SATDX\U21.JED	ARLIN		Inv	1
3	>633-0001-015	IC, AT27C010-15JC (32) (ATMEL)	U22 CS=2A2F \SPRINT\SATDX\REL0811.BIN	ARLIN		Inv	1
3	>201-0002-000	PLUG JUMPER 999-19-310-00	J8,J23,J24=1-2	ARLIN		Inv	20
3	>999-9999-001	SPECIAL NOTES	J9=5-6 7-8 11-12 13-14 17-18	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J11=1-2 3-4 (75 MHZ CPU SPEED SETTING)	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J29,J30=2-3	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J31,J32=1-3 5-6 7-9 8-10	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	*SHIPMENT JUMPERS: J28=1-2	ARLIN		Inv	1
3	>502-0010-000	HEAT SINK, BDN10-3CB	HEAT SINK, BDN10-3CB	ARLIN		Inv	1
3	>502-0009-000	HEAT SINK ADHESIVE MATERIAL,DX C	*INSTALL ONTO CPU,ADHERE WITH CONDUCTIVE	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	SYNTHETIC RESIN COATED ALUMINUM MAT'L	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	PROVIDED BY WINSYSTEMS.502-0009-000	ARLIN		Inv	1
2	910-0024-000	LABEL, STATIC SENSITIVE 130-02		ARLIN		Inv	1
2	950-0003-000	BAG PINK POLY 8X10 CHISWICK 09-0		ARLIN		Inv	1
2	910-0030-000	LABEL, AWARD BIOS	ATTACH LABEL TO BIOS AFTER PRORAMMING	ARLIN		Inv	1

9 APPENDIX E

SAT-DX Mechanical Drawing

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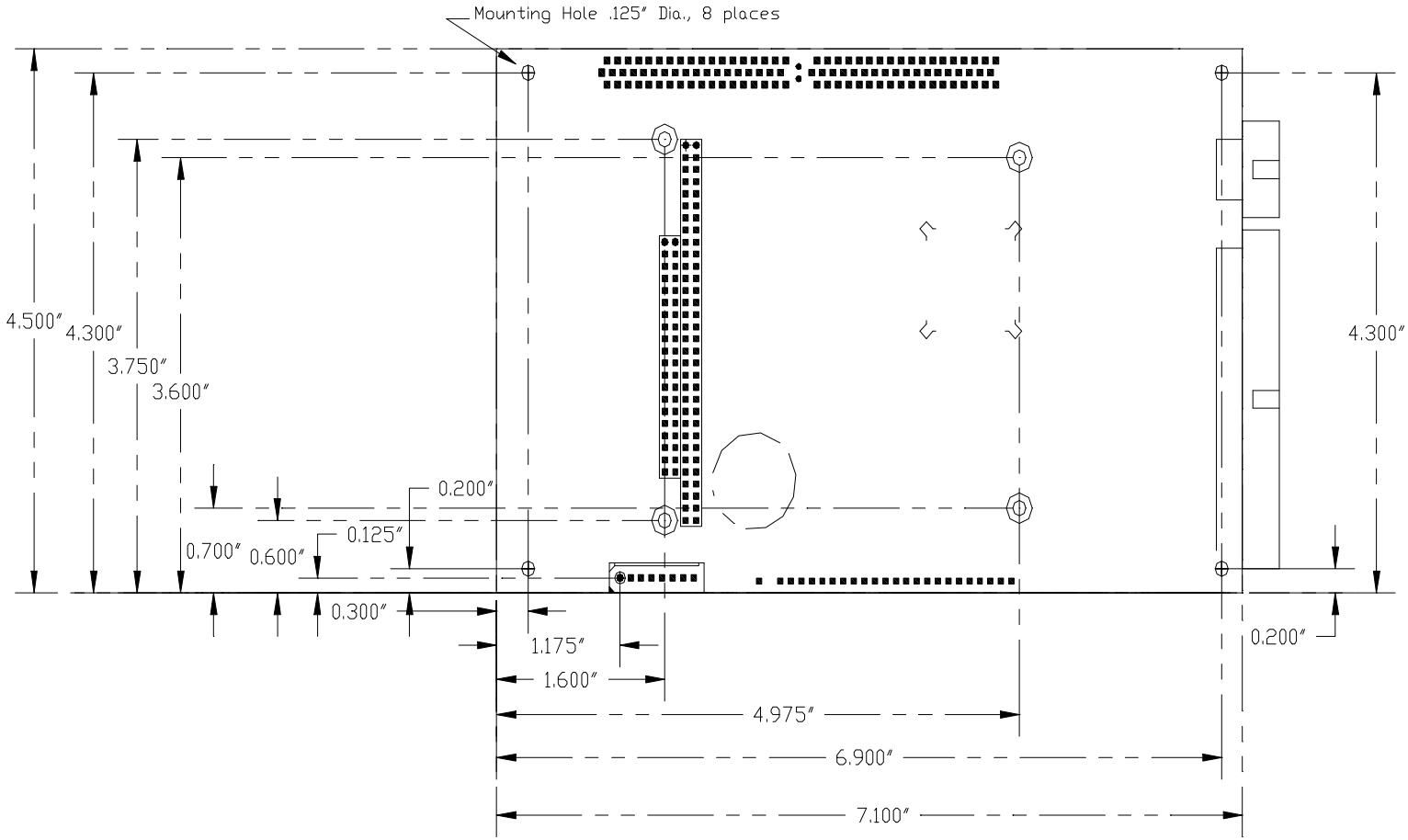
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A			



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE FRACTIONS ANGLES +/- 1/2" DECIMALS: .XX ± .03 .XXX ± .005	DRAFT/DESIGN M.BROWNING	DATE 5/03/95	*WinSystems, Inc.* "THE EMBEDDED SYSTEMS AUTHORITY"
	CHECKER	DATE	SAT-DX MOUNTING HOLES
MACHINE FINISH: √	APPROVAL	DATE	SIZE B / CAGE CODE 1AU87 / DWG NO. / REV A
	CUSTOMER APPROVAL	DATE	SCALE / CAD ID: SATSXSLC.DWG / SHEET

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10 APPENDIX F

8255 Datasheet Reprint

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μPD8255A
PROGRAMMABLE PERIPHERAL INTERFACE

Description

The μPD8255A-2 and μPD8255A-5 are general purpose programmable input/output devices designed for use with the 8080A/8085A microprocessors. Twenty-four I/O lines may be programmed in two groups of twelve (group I and group II) and used in three modes of operation. In the basic mode, (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to input or output. In the strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The bidirectional bus mode, (MODE 2), uses the 8 lines of port A for a bi-directional bus, and five lines from port C for bus control signals.

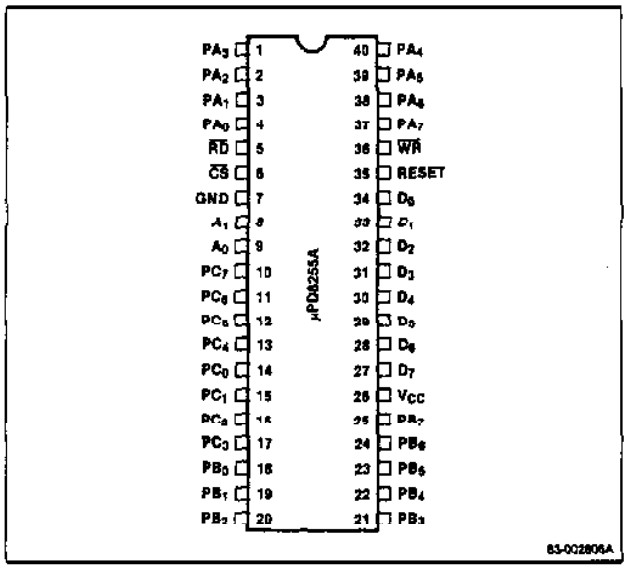
Features

- ☐ Fully compatible with the 8080A/8085 microprocessor families
- ☐ All inputs and outputs TTL compatible
- ☐ 24 programmable I/O pins
- ☐ Direct bit set/reset eases control application interfaces
- ☐ Eight Darlington drive outputs for printers and displays
- ☐ LSI drastically reduces system package count

Ordering Information

Part Number	Package Type	Max System Clock Frequency
μPD8255AC-2	40-pin plastic DIP	5 MHz
μPD8255AC-5	40-pin plastic DIP	4 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1-4, 37-40	PA_7-PA_0	Port A (I/O)
5	$\overline{RD}$	Read input
6	$\overline{CS}$	Chip select input
7	GND	Ground
8,9	A_1,A_0	Port address inputs
10-17	PC_7-PC_0	Port C (I/O)
18-25	PB_7-PB_0	Port B (I/O)
26	V_{CC}	+5 V power supply
27-34	D_7-D_0	Bidirectional data bus
35	RESET	Reset input
36	$\overline{WR}$	Write input

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Pin Functions

D_7-D_0 (Data Bus Buffer)

These pins form a three-state, bidirectional data bus buffer that is controlled by input and output instructions executed by the processor. Control words and status information are also transmitted via D_7-D_0.

$\overline{CS}$ (Chip Select)

A low input to this pin enables the μPD8255A for communication with the 8080A/8085A.

$\overline{RD}$ (Read)

A low input to this pin enables the μPD8255A for communication with the 8080A/8085A.

$\overline{WR}$ (Write)

A low input to this pin enables the data bus buffer to receive data or control words from the processor.

A_1, A_0 (Port Address)

These inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of the three ports on the control word register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor address bus.

RESET (Reset)

A high level input to this pin clears the control register and places ports A, B, and C in input mode. The input latches in ports A, B, and C are not cleared.

PA_7-PA_0, PB_7-PB_0, PC_7-PC_0 (Ports A, B, and C)

These three 8-bit I/O ports can be configured to meet a variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255A are further enhanced by special features unique to each of the ports, as follows:

- Port A has an 8-bit data output latch/buffer, data input latch/buffer, and data input latch.
- Port B has an 8-bit data I/O latch/buffer and an 8-bit data input buffer.
- Port C has an 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with ports A and B.

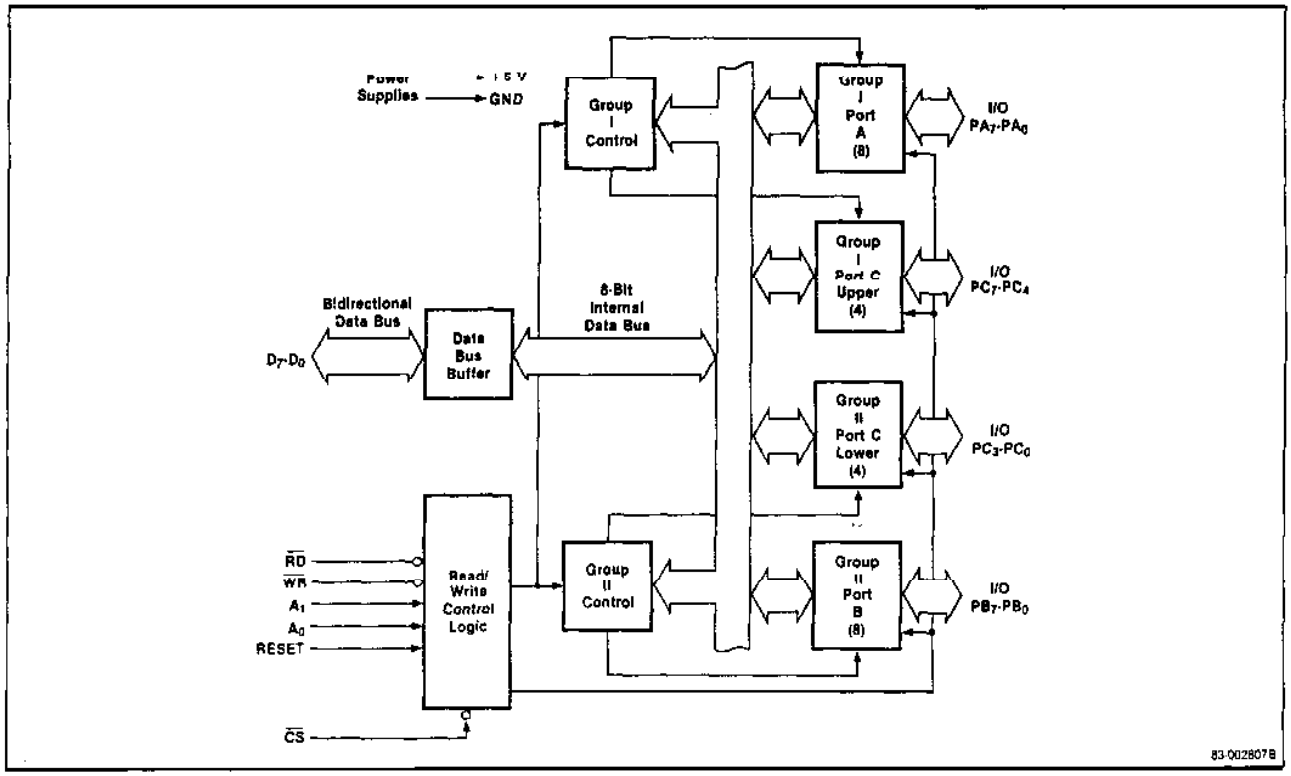
V_{CC}

+5 V power supply.

GND (Ground)

Connection to ground.

Block Diagram



Functional Description

The read/write and control logic manages all internal and external transfers of data, control, and status. It is through this block that the processor address and control buses control the peripheral interfaces.

Through an OUT instruction in system software from the processor, a control word is transmitted to the μPD8255A. Information such as the mode, bit set, and bit reset is used to initialize the functional configuration of each I/O port.

Both group I and group II accept commands from the read/write control logic and control words from the internal data bus and in turn controls its associated I/O ports, as follows:

- Group I: port A and upper port C (PC_7-PC_4)
- Group II: port B and lower port C (PC_3-PC_0)

While the control word register can be written to, the contents cannot be read back to the processor.

Absolute Maximum Ratings

T_A = 25°C

Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin with respect to V_{SS}	−0.5 to +7 V

Comment: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5 V ±10%; V_{SS} = 0 V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input low voltage	V_{IL}	−0.5	0.8	V	
Input high voltage	V_{IH}	2	V_{CC}	V	
Output low voltage	V_{OL}		0.45	V	(2)
Output high voltage	V_{OH}	2.4		V	(3)
Darlington drive current	I_{OH} (1)	−1	−4	mA	V_{EXT} = 1.5 V R_{EXT} = 750Ω
Power supply current	I_{CC}		120	mA	V_{CC} = +5 V, output open
Input leakage current	I_{LIH}		10	μA	V_{IN} = V = V_{CC}
Input leakage current	I_{LIL}		−10	μA	V_{IN} = 0.4 V
Output leakage current	I_{LOH}		±10	μA	V_{OUT} = V_{CC}; CS = 2.0 V
Output leakage current	I_{LOL}		−10	μA	V_{OUT} = 0.4 V; CS = 2.0 V

Note:

(1) Any set of eight outputs from either port A, B, C can source 4 mA into 1.5 V.

(2) I_{OL} = 2.5 mA for DB port; 1.7 mA for peripheral ports.

(3) I_{OH} = −400μA for DB port; −200 μA for peripheral ports.

Capacitance

T_A = 25°C; V_{CC} = 0V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input capacitance	C_I		10	pF	f_c = 1 MHz
I/O capacitance	C_{IO}		20	pF	Unmeasured pins returned to V_{SS}

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AC Characteristics

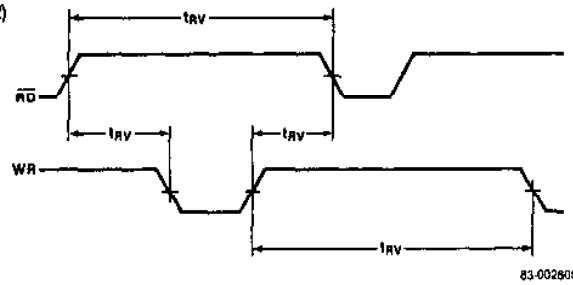
T_A = 0°C to +70°C; V_{CC} = +5 V ±5%; V_{SS} = 0 V

Parameter	Symbol	8255A-2 Limits Min	8255A-2 Limits Max	8255A-5 Limits Min	8255A-5 Limits Max	Unit	Test Conditions
Address stable before $\overline{READ}$	t_{AR}	0		0		ns	
Address stable after $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ pulse width	t_{RR}	200		250		ns	
Data valid from $\overline{READ}$	t_{RD}		140		170	ns	C_L = 150 pF
Data float after $\overline{READ}$	t_{DF}		100		100	ns	C_L = 100 pF
		10		10		ns	C_L = 15 pF
Time between $\overline{READ}$s and /$\overline{WRITE}$s	t_{RV}	200		850		ns	(Note 2)
Write							
Address stable before $\overline{WRITE}$	t_{AW}	0		0		ns	
Address stable after $\overline{WRITE}$	t_{WA}	20		20		ns	
$\overline{WRITE}$ pulse width	t_{WW}	200		250		ns	
Data valid to $\overline{WRITE}$ (T.E.)	t_{DW}	100		100		ns	
Data valid after $\overline{WRITE}$	t_{WD}	0		0		ns	
Other Timing							
$\overline{WR}$ = 0 to output	t_{WB}		350		350	ns	C_L = 150 pF
Peripheral data before $\overline{RD}$	t_{IR}	0		0		ns	
Peripheral data after $\overline{RD}$	t_{HR}	0		0		ns	
$\overline{ACK}$ pulse width	t_{AK}	300		300		ns	
$\overline{STB}$ pulse width	t_{ST}	350		350		ns	
Per. data before T.E. of $\overline{STB}$	t_{PS}	0		0		ns	
Per. data after T.E. of $\overline{STB}$	t_{PH}	150		150		ns	
$\overline{ACK}$ = 0 to output	t_{AD}		300		300	ns	C_L = 150 pF
$\overline{ACK}$ = 0 to output float	t_{KD}		250		250	ns	C_L = 50 pF
		20		20			C_L = 15 pF
$\overline{WR}$ = 1 to OBF = 0	t_{WOB}		300		650	ns	
$\overline{ACK}$ = 0 to OBF = 1	t_{AOB}		350		350	ns	
$\overline{STB}$ = 0 to IBF = 1	t_{SIB}		300		300	ns	
$\overline{RD}$ = 1 to IBF = 0	t_{RIB}		300		300	ns	
$\overline{RD}$ = 0 to INTR = 0	t_{RIT}		400		400	ns	
$\overline{STB}$ = 1 to INTR = 1	t_{SIT}		300		300	ns	C_L = 150 pF
$\overline{ACK}$ = 1 to INTR = 1	t_{AIT}		350		350	ns	
$\overline{WR}$ = 0 to INTR = 0	t_{WIT}		450		850	ns	C_L = 150 pF (Note 3)

Note:

(1) Period of reset pulse must be at least 50 μs during or after power on. Subsequent reset pulse can be 500 ns min.

(2)



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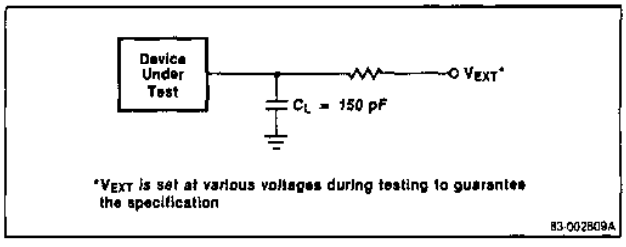
(3) INTR↑ may occur as early as $\overline{WR}$↓.

AC Testing Load Circuit



*V_{EXT} is set at various voltages during testing to guarantee the specification

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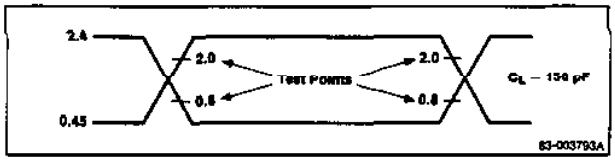
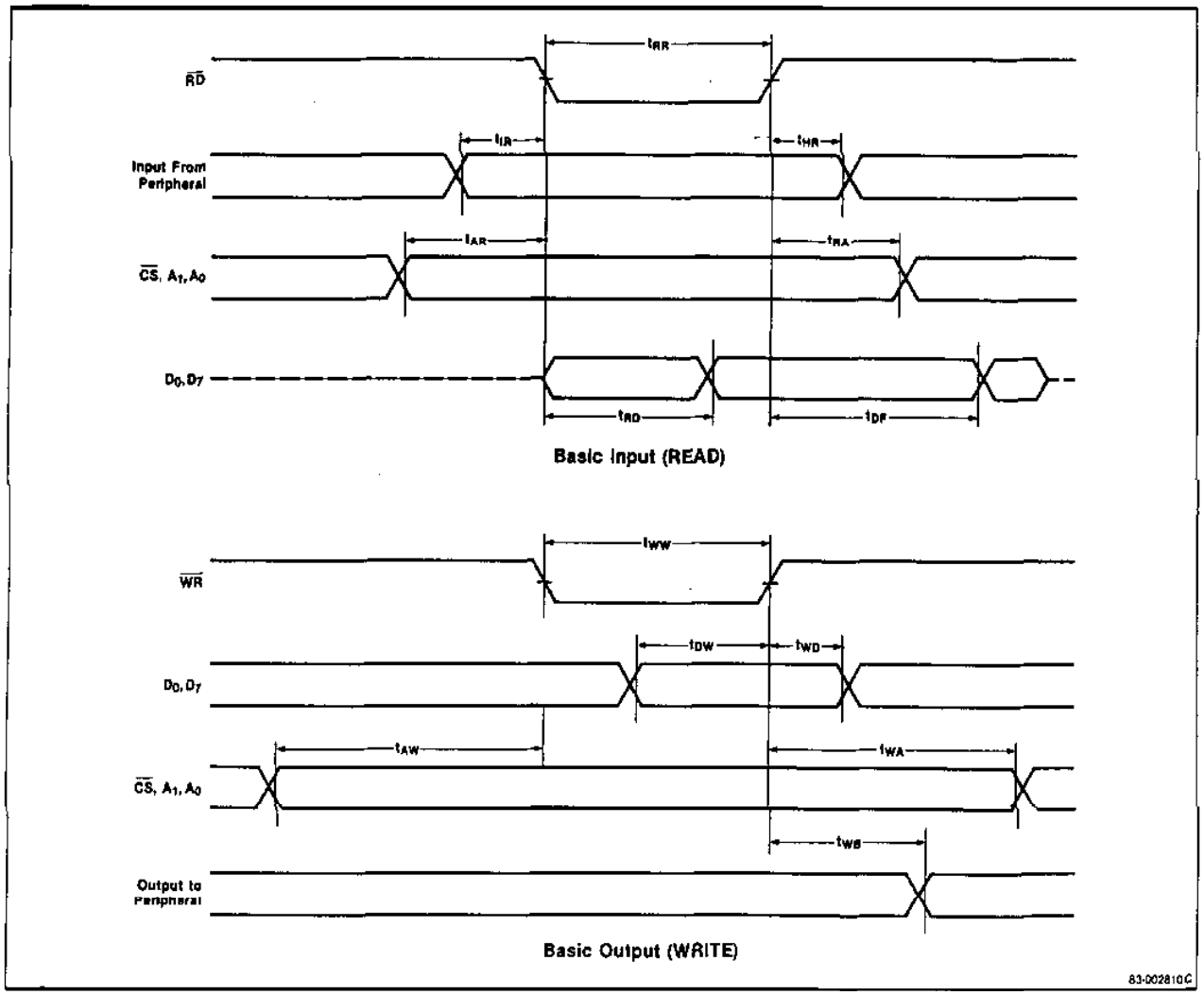
Timing Waveforms

AC Testing Input, Output Waveform



Mode 0



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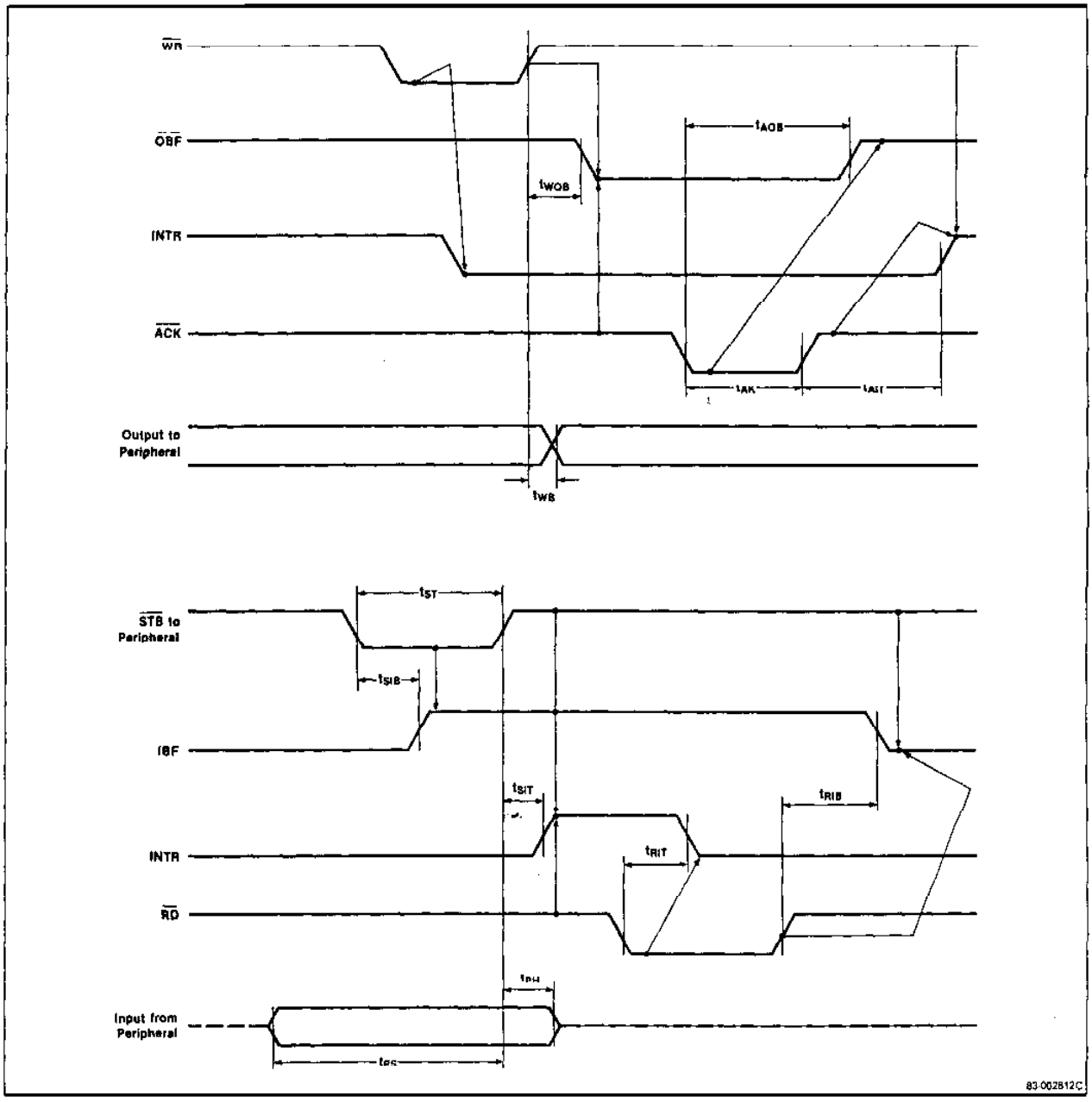
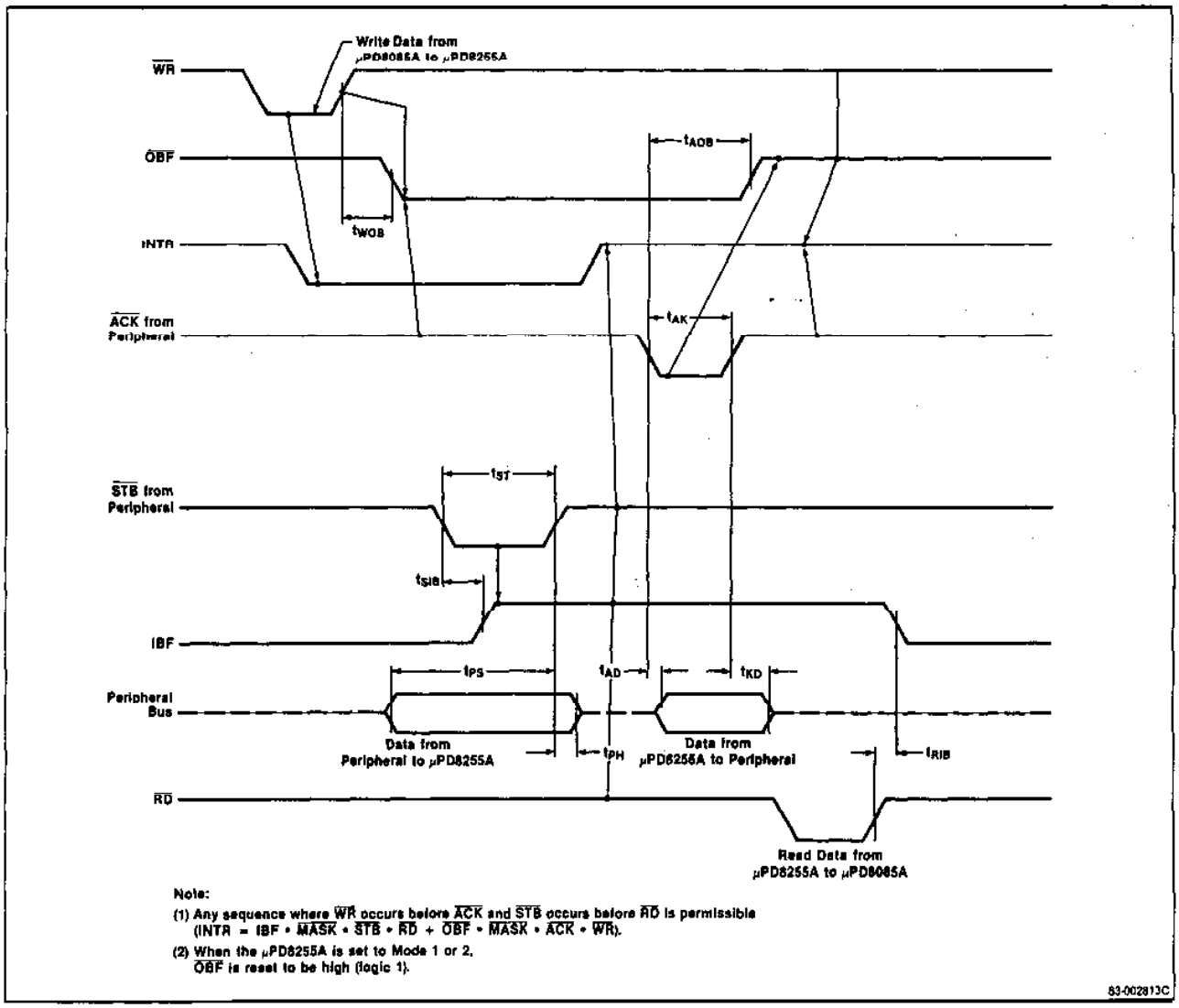
Timing Waveforms (cont)

Mode 1



Timing Waveforms (cont)

Mode 2



Note:

(1) Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$).

(2) When the μPD8255A is set to Mode 1 or 2, $\overline{OBF}$ is reset to be high (logic 1).

83-002813C

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Modes

The μPD8255A can be operated in modes 0, 1 or 2 which are selected by appropriate control words and are detailed below.

Mode 0

Mode 0 provides basic input and output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.

- 16 different configurations in mode 0
- Two 8-bit ports and two 4-bit ports
- Inputs are not latched
- Outputs are latched

Mode 1

Mode 1 provides for strobed input and output operations with data transferred through port A or B and handshaking through port C.

- Two I/O groups (I and II)
- Both groups contain an 8-bit data port and a 4-bit control/data port
- Both 8-bit data ports can be either latched input or latched output

Mode 2

Mode 2 provides for strobed bidirectional operation using PA_0PA_7 as the bidirectional latched data bus. PC_3PC_7 is used for interrupts and "handshaking" bus flow control similar to mode 1. Note that PB_0PB_7 and PC_0PC_2 may be defined as mode 0 or 1, input or output in conjunction with port A in mode 2.

- An 8-bit latched bidirectional bus port (PA_0-PA_7) and a 5-bit control port (PC_3PC_7)
- Both inputs and outputs are latched
- An additional 8-bit input or output port with a 3-bit control port.

Basic Operation

Input Operation (Read)

A_1	A_0	RD	WR	CS	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

Output Operation (Write)

A_1	A_0	RD	WR	CS	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

Disable Function

A_1	A_0	RD	WR	CS	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

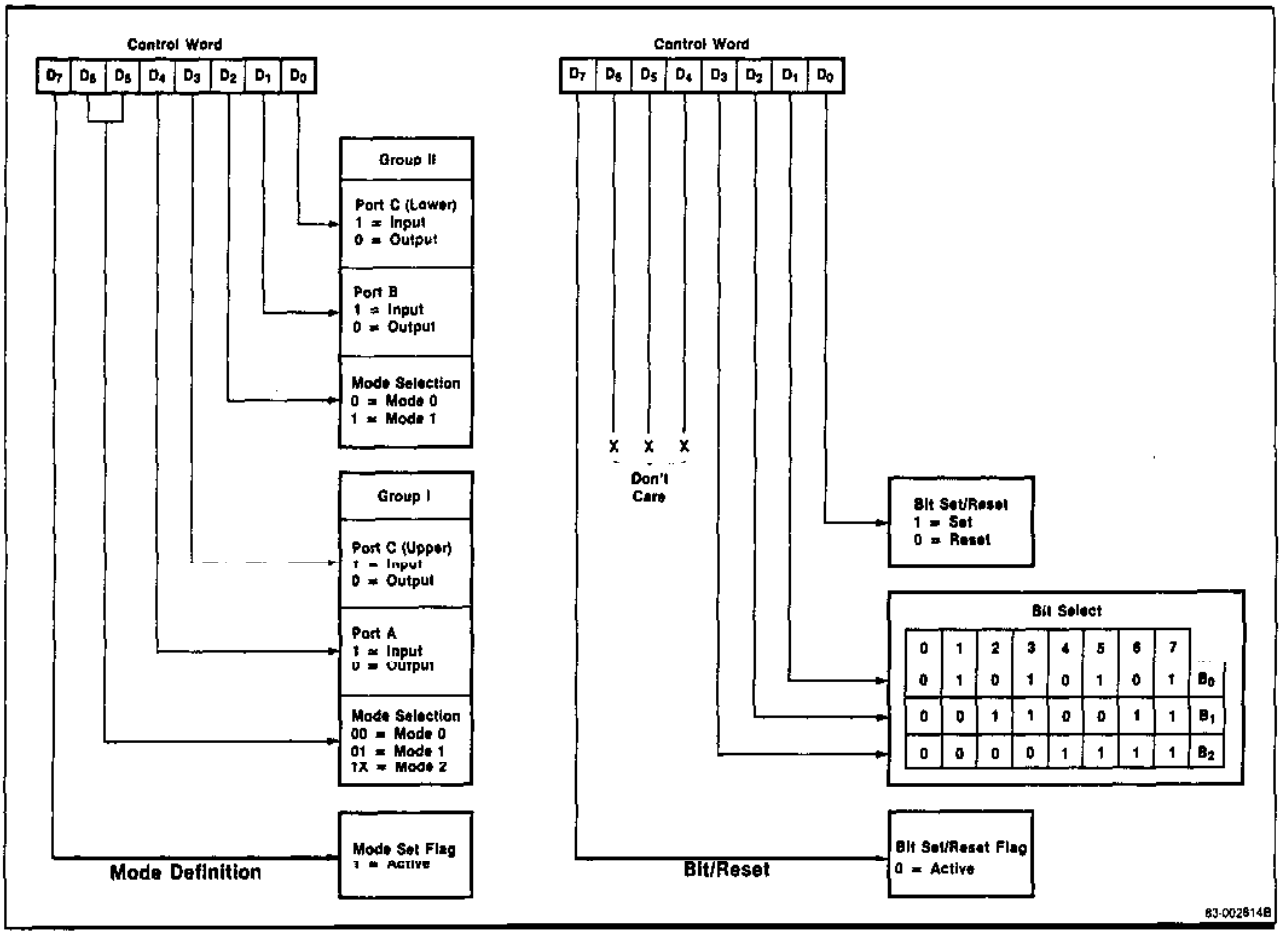
Note:

(1) X means "DO NOT CARE"

(2) All conditions not listed are illegal and should be avoided.

Formats

Mode Definition, Bit/Rest Format



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