OPERATIONS MANUAL
EPX-855

NOTE: *This manual has been designed and created for use as part of WinSystems Technical Manuals CD and/or the WinSystems website. If this manual or any portion of the manual is downloaded, copied or emailed, the links to additional information (i.e. software, cable drawings) may be inoperable.*

REVISION HISTORY

P/N 400-0347-000

Revision Date Code	ECO Number
090115	Preliminary
100521	
130708	

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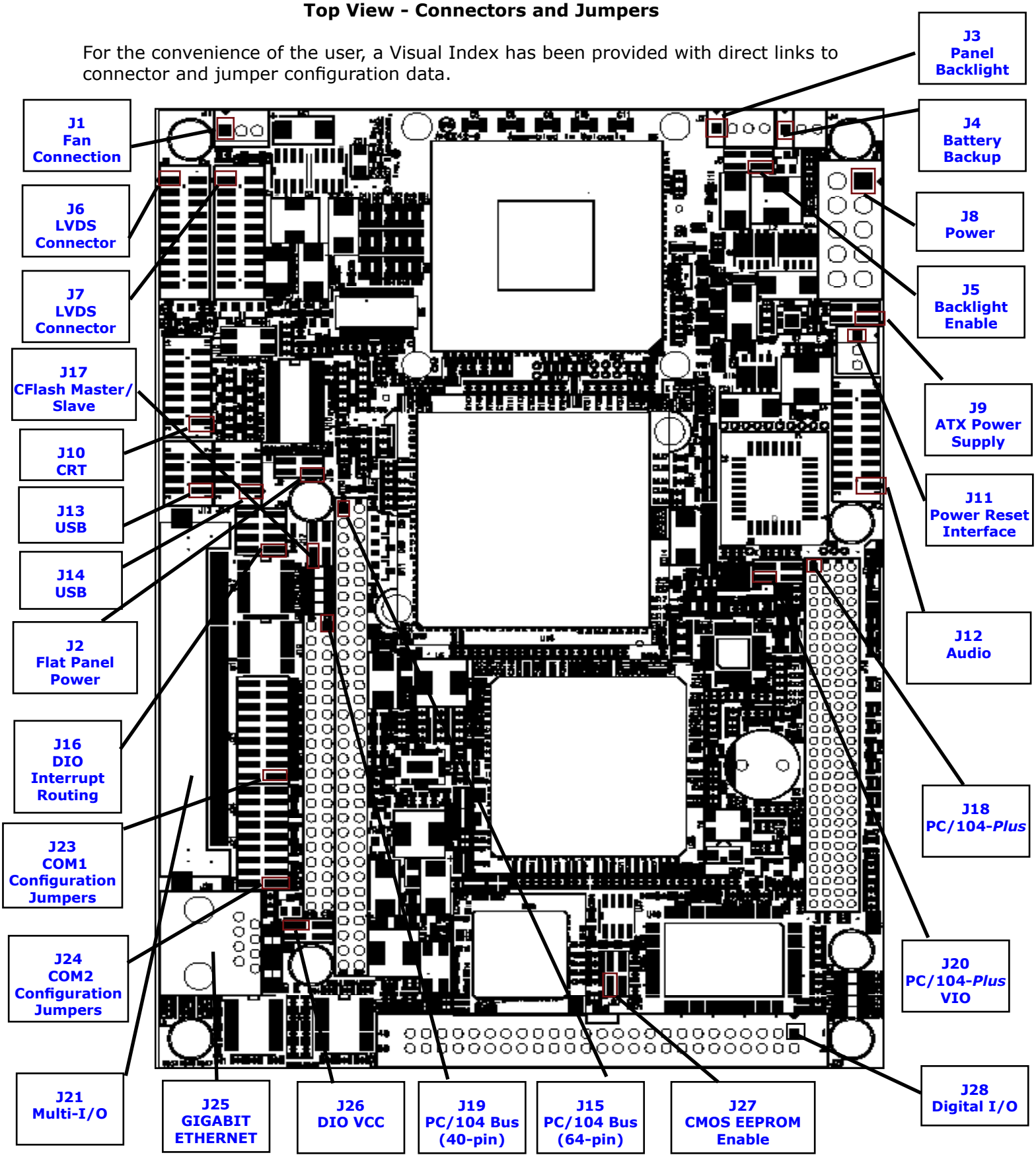
Visual Index – Quick Reference

Top View - Connectors and Jumpers

For the convenience of the user, a Visual Index has been provided with direct links to connector and jumper configuration data.

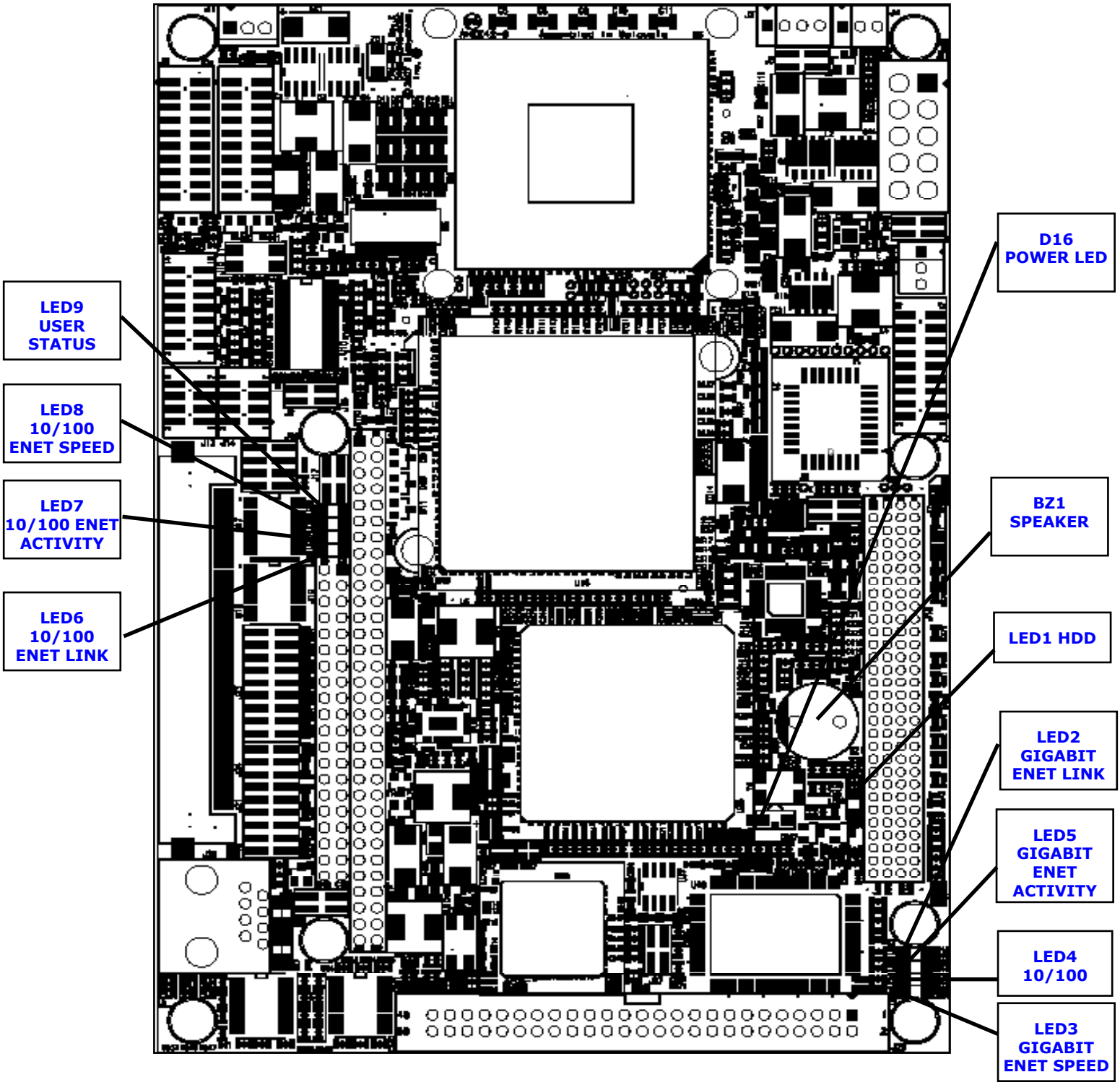


NOTE: The reference line to each component part has been drawn to Pin 1, where applicable. Pin 1 is also highlighted with a red square, where applicable.

Visual Index – Quick Reference

Top View - LEDS

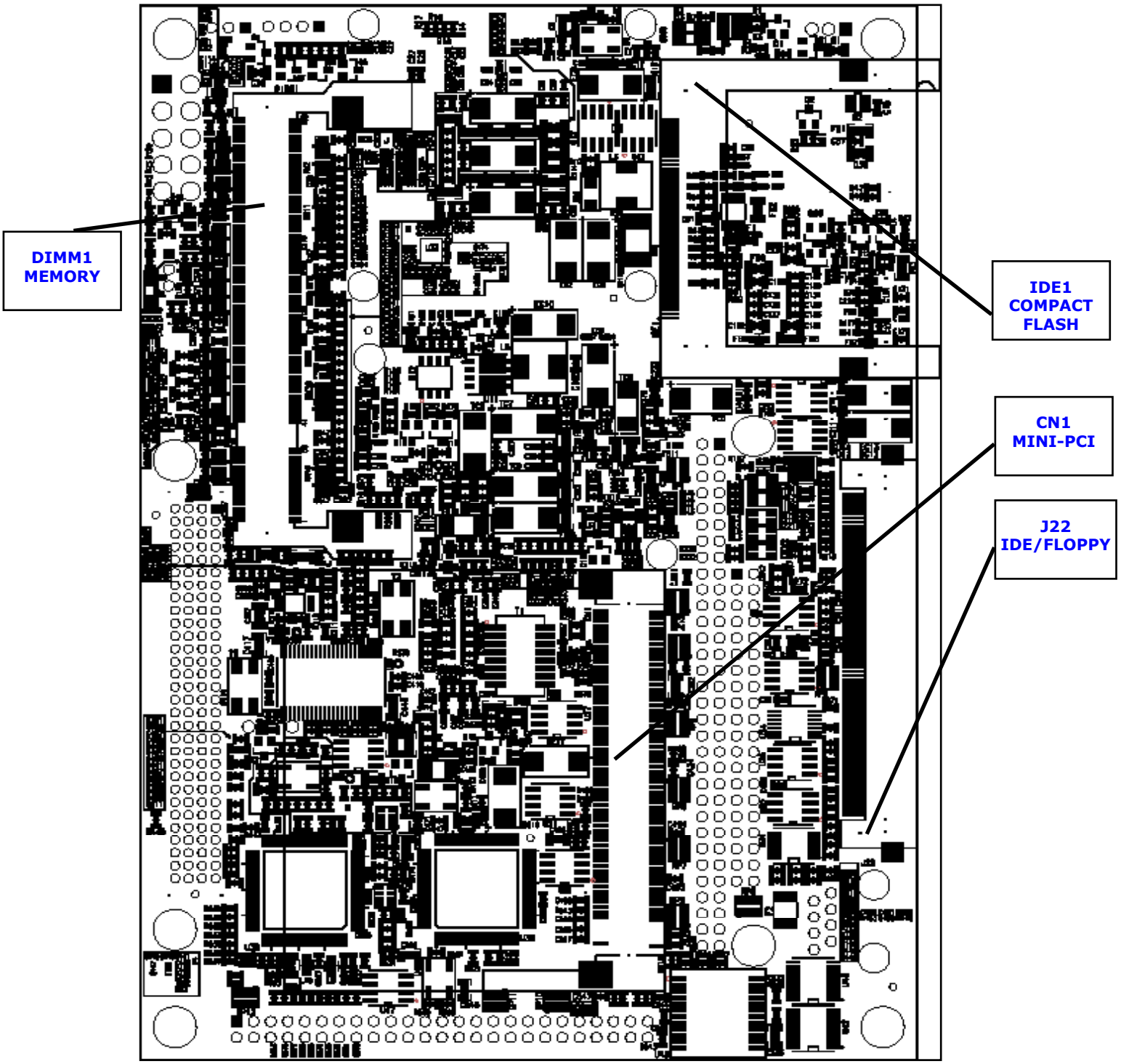
For the convenience of the user, a Visual Index has been provided with direct links to connector and jumper configuration data.



Visual Index – Quick Reference

Bottom View

For the convenience of the user, a Visual Index has been provided with direct links to connector and jumper configuration data.



Introduction

This manual is intended to provide the necessary information regarding configuration and usage of the EPX-855 board. WinSystems maintains a Technical Support Group to help answer questions regarding usage or programming of the board. For answers to questions not adequately addressed in this manual, contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

General Information

Features

Processor
- Intel® 1 GHz ZCD™
- Intel® 1.8 GHz Pentium M™

Operating Systems Supported
- x86 RTOS, XP Embedded, Linux, DOS

Memory
- Up to 1028 MB of 200-pin SODIMM PC2700 DDR SDRAM (Socketed)

Video
- Up to 2048x1536 resolution

Ethernet
- Intel DA82562ET 10/100 Mbps controller (8255x compatible)
- Intel 82541ER 10/100/1000 Mbps controller

Wireless
- IEEE 802.11a/b/g via a miniPCI socket

Digital I/O
- 24 Bidirectional lines (WS16C48)

Serial I/O
- Four (4) serial ports (Two(2)-RS-232, Two(2)-RS-232/422/485)

Line Printer Port
- SPP/EPP/ECP supported

USB
- Four (4) USB 2.0 ports

Interrupts
- Two (2) interrupt controllers
- Seven (7) DMA channels

Watchdog Timer
- Up to 300 second reset

CompactFlash
- Types I & II supported

IDE
- Two (2) IDE ports

Floppy Drive
- One (1) 3.5” drive supported

Power
- +5V required, 2.1A typical *(+5V required, 4.25A typical for Intel® 1.8 GHz Pentium M™)

Industrial Operating Temperature Range
- -40°C to 70°C (1.8 GHz Pentium M™ with fan)
- -40°C to 70°C (1 GHz ZCD™ without fan)
- -40°C to 85°C (1 GHz ZCD™ with fan)

Form Factor
- EPIC-compliant
- 4.50” x 6.5” (115 mm x 165 mm)

Additional Features
- RoHS compliant (meets EU directive 2002/95/EC)
- PC/104 and PC/104-*Plus* expansion connectors
- Phoenix® BIOS
- Backlight power supported
- Custom splash screen on start up
- Real-time clock
- Simultaneous CRT and LVDS flat panel supported
- Activity status LEDs onboard
- AC97 Support
- PS/2 Keyboard Supported
- PS/2 Mouse Supported

Software Support

The EPX-855 is an x86-compatible SBC. The architecture of the EPX-855 is designed to run standard x86 operating systems. Commonly used operating systems include XPe, DOS, Linux and other operating systems such as QNX or VxWorks. Its x86-PC software compatibility assures a wide range of tools to aid in developing and checkout of your application’s program.

Software Developers Kit

WinSystems offers software developers kits to provide the necessary hardware, software and cables to aid program development with the EPX-855 board. The configuration consists of an operating system, DVD-ROM drive, a hard disk, a 3.5” floppy disk, plus the required cables and a triple output power supply housed in an enclosure. This packaging permits easy access to the board, PC/104 modules and peripherals during program development.

Functional Capability

System Processor

The EPX-855 is based upon the Intel Pentium M or Zero Cache Dothan (ZCD) CPU which supports two speeds: Pentium M 1.8 GHz and ZCD 1.0 GHz. It uses a Micro-FCBGA Package of 479-pins based on 90 nm process technology featuring up to 2 MB L2 Cache and 400 MHz Front-Side Bus(FSB).

System Controllers

The Intel 855GME chipset which interfaces to the CPU, DDR SDRAM memory and the graphics interface. The memory system supports 200/266/333 MHz DDR SDRAM device (up to 1 GB). There is also a graphics controller with LVDS and CRT support.

The Intel Chipset ICH4 provides many I/O features. It contains two IDE ports – Primary (HDD) and Secondary (CF) with ATA100, audio codec AC97, four USB ports (2.0), SM Bus, LAN link to Intel Ethernet controller, general purpose I/O ports, low pin count (LPC) bus interface, PCI Bus interface, Real-Time Clock (RTC), watchdog timer and power management.

Memory

The EPX-855 can support a maximum of 1 GB of RAM with the 200-pin SODIMM socket located on the back of the board at **DIMM1**.

Qualified SODIMMS are available directly from WinSystems. WinSystems cannot guarantee the operation of systems using nonqualified SODIMM modules.

The RAM can be user supplied, but must meet the following criteria:

200-Pin SODIMM PC2700 DDR SDRAM with gold fingers (up to 1 GB)

Installation is accomplished by inserting the module into the connector at approximately a 30 degree angle. Press firmly to fully seat the module into the connector and then press the module downward to snap it into the retaining clamps.

Removal is accomplished by gently pulling outward on the retaining clamps until the module springs up to the appropriate removal angle.

DMA

DMA is supported. Channel 2 is dedicated to the floppy disk controller. The LPT is plug-and-play configurable. The other 8-bit DMA channels are wired to the PC/104 connector. 16-bit transfers are not supported.

Interrupt Routing

All interrupts are routed to their respective PC/104 bus pins. The Digital I/O is the only interrupt routing that is jumper selectable at **J16**. For further details, refer to the Digital I/O Section later in this manual.

Power and Reset Interface

Power is applied to the EPX-855 via the connector at **J8** (Molex part number 26-60-7091). The pin definitions for **J8** are given below. An optional push-button-reset (normally OPEN) may also be routed into **J11,** pin 1-2 if desired. Momentary closure to ground forces a hardware reset.

J8	+5VSB	**6 o o 1**	PS_ON
	+5V	**7 o o 2**	GND
	+5V	**8 o o 3**	GND
	-12V	**9 o o 4**	+12V
	GND	**10 o o 5**	+3.3V*

* - **only connects to the PC/104-*Plus* connector**

Power Supply Selection

The EPX-855 supports either AT (standard power supply) or ATX type power supplies. Zero load supplies are recommended. **J9** specifies the style of supply connected to the single board computer (SBC). An AT power supply is a simple on/off supply with no interaction with the single board computer. Most embedded systems use this type of power supply and it is the default setting.

ATX type power supplies function with a "soft" on/off power button and a +5 VSB (standby). If an ATX compatible power supply is connected, **J9** should be set accordingly and a power button (momentary contact) connected between pin 3 (power button) and pin 2 (ground) of **J11**. The +5 VSB signal on **J8** provides the standby voltage to the EPX-855 but does not power any other features of the board. When the power button is pressed, the EPX-855 pulls PSON (Power Supply On) low and the power supply turns on all voltages to the single board computer. When the power button is pressed again, the BIOS signals the event so ACPI-compliant operating systems can be shutdown before the power is turned off. Since this is software driven, it is possible that a software lockup could prevent the power button from functioning properly. For the BIOS to report the ATX supply to ACPI-compatible operating systems, **J9** must be setup correctly.

NOTE: True ATX power supplies are not applicable for embedded systems. They are typically 300W supplies and may not regulate properly with low power embedded systems such as the EPX-855.

J9	**4 o o 3** **2 o o 1**	1-2, 3-4 = AT 1 2, 3 4 = ATX

J11	**1 o** **2 o** **3 o**	RESET GND PWRBTN

Power LED

An on-board LED, located at **D16**, indicates the state of the system as reflected in this table.

LED	Description
OFF	Power OFF Mode
GREEN	Operating Mode
AMBER	Standby Mode

Power Fail Reset

A precision voltage comparator monitors the +5V status. The out-of-tolerance value is 4.45V ±0.15V. Upon detection of an out-of-tolerance condition, the board is reset. This action is critically important in order to detect brownout or power fail conditions. The reset circuit also ensures that the power is nominal before executing a power-on reset. This circuit also inhibits the processor's memory write line, preventing invalid data from being written to nonvolatile memory during power fluctuations.

BIOS

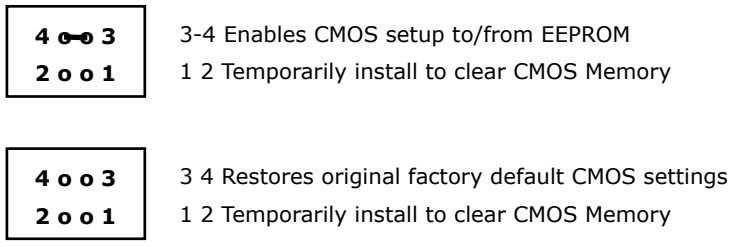
The EPX-855 BIOS provides configuration flexibility, performance and PC-compatibility. Specific BIOS-related information can be found in the BIOS Supplemental to be released in later versions of this manual.

Saving BIOS Setup

The EPX-855 provides two methods for saving BIOS setup data:
Standard battery backed CMOS RAM and **Nonvolatile EEPROM**.

The battery is enabled/disabled using connector **J4**. For further details, refer to the Battery Backup Section later in this manual.

The EEPROM write/read functionality is enabled/disabled at **J27**, pins 3 and 4.



Real-Time Clock/Calendar

A real-time clock (RTC) is used as the PC-compatible clock/calendar. It supports a number of features, including periodic and alarm interrupt capabilities. In addition to the time and date keeping functions, the system configuration is kept in CMOS RAM contained within the clock section.

Battery Backup

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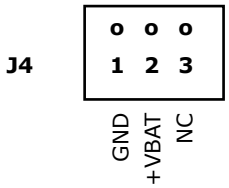
A connector is available at **J4** to provide battery backup to the real-time clock and CMOS. The battery input voltage range is 3.0V to 3.6V, ±5%. An extended temperature lithium battery capable of backing up the EPX-855 RTC and CMOS is available from WinSystems, part number BAT-LTC-E-36-27-1 (2.7A) or BAT-LTC-E-36-16-1 (1.6A). Contact your WinSystems' Applications Engineer for additional information.



(Provides battery backup to RTC and BIOS CMOS.)

WARNING: BAT-LTC-E-36-27-1 (or BAT-LTC-E-36-16-1 if applicable) must be connected at J4. Improper connection may result in explosive failure. It is possible for the battery to violently explode if installed incorrectly. Please be careful to note correct connection at location J4.

Rotational Disk Support

IDE Support

An industry standard UDMA/100 capable 16-bit IDE controller is provided to support up to two hard disks. A status LED, **LED1**, provides visual status during IDE data transfers. The 40-pin primary IDE controller interface is provided at the 80-pin header **J22**. CompactFlash is available on the secondary IDE controller. WinSystems offers cable CBL-252-G-1-1.5 (80-pin) to simplify the connection to the primary IDE interface as well as the floppy disk interface.

J22

RESET	**A1 o o B1**	GND
GND	**A2 o o B2**	DRVEND0
D7	**A3 o o B2**	GND
D8	**A4 o o B4**	NC
D6	**A5 o o B5**	GND
D9	**A6 o o B6**	NC
D5	**A7 o o B7**	GND
D10	**A8 o o B8**	NIDEX
D4	**A9 o o B9**	GND
D11	**A10 o o B10**	RT0
D3	**A11 o o B11**	GND
D12	**A12 o o B12**	NC
D2	**A13 o o B13**	GND
D13	**A14 o o B14**	NDS0
D1	**A15 o o B15**	GND
D14	**A16 o o B16**	NC
D0	**A17 o o B17**	GND
D15	**A18 o o B18**	NDIR
GND	**A19 o o B19**	GND
NC	**A20 o o B20**	NSTEP
REQ	**A21 o o B21**	GND
GND	**A22 o o B22**	NWDATA
IOW#	**A23 o o B23**	GND
GND	**A24 o o B24**	NWGATE
IOR#	**A25 o o B25**	GND
GND	**A26 o o B26**	NTRK0
IORDY	**A27 o o B27**	GND
NC	**A28 o o B28**	NWRTPRT
DACK#	**A29 o o B29**	GND
GND	**A30 o o B30**	NRDATA
IRQ14	**A31 o o B31**	GND
NC	**A32 o o B32**	NHDSEL
PDA1	**A33 o o B33**	GND
DET	**A34 o o B34**	NDSKCHG
PDA0	**A35 o o B35**	GND
PDA2	**A36 o o B36**	NC
PDSC1#	**A37 o o B37**	USB_0C4#
PDCS3#	**A38 o o B38**	USBD4-
ACT#	**A39 o o B39**	USBD4+
GND	**A40 o o B40**	+5V

CompactFlash

The EPX-855 supports bootable solid state CompactFlash storage devices for applications where the environment is too harsh for mechanical hard disks or floppy drives. The socket is on the secondary IDE controller.

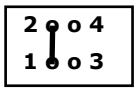
The CompactFlash socket at **IDE1**, on the back of the board, supports modules with TrueIDE support. WinSystems offers industrial grade CompactFlash modules that provide high performance and extended temperature operation (-40ºC to +85ºC). An IDE activity LED is present at **LED1**. Also, one, 3.5" floppy disk drive is also supported at **J22**.

IDE1

GND	**1 o o 2**	D3
D4	**3 o o 4**	D5
D6	**5 o o 6**	D7
HDCS0	**7 o o 8**	GND
GND	**9 o o 10**	GND
GND	**11 o o 12**	GND
CFVCC	**13 o o 14**	GND
GND	**15 o o 16**	GND
GND	**17 o o 18**	A2
A1	**19 o o 20**	A0
D0	**21 o o 22**	D1
D2	**23 o o 24**	N/C
N/C	**25 o o 26**	N/C
D11	**27 o o 28**	D12
D13	**29 o o 30**	D14
D15	**31 o o 32**	HDCS1
GND	**33 o o 34**	IOR
IOW	**35 o o 36**	CFWE
IRQ	**37 o o 38**	CFVCC
Slave/Master	**39 o o 40**	N/C
Reset	**41 o o 42**	RDY
SDDREQ	**43 o o 44**	DACK
LED	**45 o o 46**	N/C
D8	**47 o o 48**	D9
D10	**49 o o 50**	GND

When using a CompactFlash device, Master/Slave selection is made using jumper field **J17.**

CFLASH (J17)



3 4 not used

1-2 CFlash Master, 1 2 CFlash Slave

Multi-I/O Connector

The I/O to the primary serial channels, the 10/100 Mbps Ethernet controller, the printer port, keyboard and mouse are all terminated via a high-density connector at **J21**. An adapter cable, part number CBL-251-G-2-1.0, is available from WinSystems to adapter to the conventional I/O connectors. The pin definitions for **J21** are shown below.

NOTE: Pins 1-9 are used for COM1, pins 10-18 are used for COM2, 19-27 are used for COM3, and pins 29-36 are used for COM4. Pin definitions for use as RS-232, RS-422 or RS-485 are shown in the Serial Interface section of this manual.

J21

STROBE (LPT)	**A1 o o B1**	(COM1) DCD
AUTOFD (LPT)	**A2 o o B2**	(COM1) DSR
PD0 (LPT)	**A3 o o B2**	(COM1) RX
ERROR (LPT)	**A4 o o B4**	(COM1) RTS
PD1 (LPT)	**A5 o o B5**	(COM1) TX
INIT (LPT)	**A6 o o B6**	(COM1) CTS
PD2 (LPT)	**A7 o o B7**	(COM1) DTR
SLCTIN (LPT)	**A8 o o B8**	(COM1) RI
PD3 (LPT)	**A9 o o B9**	(COM1) GND
GND (LPT)	**A10 o o B10**	(COM2) DCD
PD4 (LPT)	**A11 o o B11**	(COM2) DSR
GND (LPT)	**A12 o o B12**	(COM2) RX
PD5 (LPT)	**A13 o o B13**	(COM2) RTS
GND (LPT)	**A14 o o B14**	(COM2) TX
PD6 (LPT)	**A15 o o B15**	(COM2) CTS
GND (LPT)	**A16 o o B16**	(COM2) DTR
PD7 (LPT)	**A17 o o B17**	(COM2) RI
GND (LPT)	**A18 o o B18**	(COM2) GND
ACK (LPT)	**A19 o o B19**	(COM3) DCD
GND (LPT)	**A20 o o B20**	(COM3) DSR
BUSY (LPT)	**A21 o o B21**	(COM3) RX
GND (LPT)	**A22 o o B22**	(COM3) RTS
PE (LPT)	**A23 o o B23**	(COM3) TX
GND (LPT)	**A24 o o B24**	(COM3) CTS
SLCT (LPT)	**A25 o o B25**	(COM3) DTR
RX+ (ETH)	**A26 o o B26**	(COM3) RI
RX-(ETH)	**A27 o o B27**	(COM3) GND
TX+ (ETH)	**A28 o o B28**	(COM4) DCD
TX-(ETH)	**A29 o o B29**	(COM4) DSR
LED6 (LINK*)	**A30 o o B30**	(COM4) RX
LED7 (ACT*)	**A31 o o B31**	(COM4) RTS
LED8 (SPEED*)	**A32 o o B32**	(COM4) TX
LED9 (USER*)	**A33 o o B33**	(COM4) CTS
+5V	**A34 o o B34**	(COM4) DTR
RESET	**A35 o o B35**	(COM4) RI
GND	**A36 o o B36**	(COM4) GND
MDAT (MOUSE)	**A37 o o B37**	(KYBD) KCLK
GND (MOUSE)	**A38 o o B38**	(KYBD) KDAT
+5V(MOUSE)	**A39 o o B39**	(KYBD) GND
MCLK (MOUSE)	**A40 o o B40**	(KYBD) +5V

* - For Active Low LED Outputs

Serial Interface

Four independent, full-duplex, 16C550 compatible, RS-232 asynchronous serial channels are on-board the EPX-855. All serial channels (COM1, COM2, COM3 and COM4) are terminated at **J21,** the 80-pin Multi-I/O high density connector, and can be configured for RS-232 (COM1/COM2/COM3/COM4), RS-485(COM1/COM2) or RS-422 (COM1/COM2). An adapter cable, part number CBL-251-G-2-1.0, is available from WinSystems to adapt to the conventional I/O connectors. The pinouts for the connector and cable, as well as connector variations for RS-232, RS-422 and RS-485 follow. For additional information on cable connection, refer to the Multi-I/O section of this manual.

J21 – COM1/COM2 80-pin Multi-I/O Connector

COM1

RS-485	RS-422	RS-232	J21 Pin#	RS-232	RS-422	RS-485
N/A	N/A	DCD	B 1-2	DSR	RX+	N/A
TX/RX+	TX+	RXD	B 3-4	RTS	RX+	N/A
TX/RX-	TX-	TXD	B 5-6	CTS	N/A	N/A
N/A	N/A	DTR	B 7-8	RI	N/A	N/A
GND	GND	GND	B 9			

COM2

RS-485	RS-422	RS-232	J21 Pin#	RS-232	RS-422	RS-485
			B 10	DCD	N/A	N/A
N/A	RX+	DSR	B 11-12	RXD	TX+	TX/RX+
N/A	RX-	RTS	B 13-14	TXD	TX-	TX/RX-
N/A	N/A	CTS	B 15-16	DTR	N/A	N/A
N/A	N/A	RI	B 17-18	GND	GND	GND

J21 – COM3/COM4 80-pin Multi-I/O Connector (RS-232 Only)

COM3

RS-232	J21 Pin#	RS-232
DCD	B 19-20	DSR
RXD	B 21-22	RTS
TXD	B 23-24	CTS
DTR	B 25-26	RI
GND	B 27	

COM4

RS-232	J21 Pin#	RS-232
	B 28	DCD
DSR	B 29-30	RXD
RTS	B 31-32	TXD
CTS	B 33-34	DTR
RI	B 35-36	GND

COM1 and COM2 Configuration
COM1 and COM2 addresses and interrupts are set using the BIOS CMOS setup. Both COM1 and COM2 can be individually configured for any one of the following operating modes:

1. RS-232 Mode
2. RS-422 Mode with RTS transmitter enable
3. RS-422 Mode with auto transmitter enable
4. RS-485 Mode with RTS transmitter enable
5. RS-485 Mode with RTS transmitter enable and echo back
6. RS-485 Mode with auto transmitter enable
7. RS-485 Mode with auto transmitter enable and echo back

Modes 2, 4 and 5 require the RTS bit (MCR Bit 1) be set in order to Transmit.
Modes 4 and 5 require that RTS (MCR Bit 1) be de-asserted in order to receive.

Each of the RS-422/RS-485 modes allow for jumper selection of transmit and/or receive termination resistor(s). There is an 11-pin configuration jumper for COM1 and COM2 that allows the user to select the operating mode and its optional features and termination. The jumper numbers and corresponding port numbers are shown on the following pages. There are three choices for termination when RS-422 or RS-485 modes are used.

TX(100) : Places a 100Ω resistor across the **TX+/TX-** pair

RX(100) : Places a 100Ω resistor across the **RX+/RX-** pair

TX/RX(300) : Places a 100Ω Resistor from +5V to **TX/RX+**, a 100Ω resistor from **TX/RX-** to ground and a 100Ω resistor between **TX/RX+** and **TX/RX-**.

COM1 is configured by setting jumpers at **J23** and COM2 is configured by setting jumpers at **J24**, as shown in the tables below. The tables provide the appropriate jumpering for the various modes.

COM1

Mode #	Description	J23	Termination J23		
			TX (100)	RX (100)	TX/RX (300)
1	RS-232	1-2	N/A	N/A	N/A
2	RS-422 RTS ENABLE	3-4 9-10	13-14	17-18	11-12 13-14 15-16
3	RS-422 AUTO ENABLE	3-5, 9-10 (One node must use TX-RX 300 Termination)	N/A	17-18	11-12 13-14 15-16
4	RS-485 RTS ENABLE	3-4, 7-8	13-14	N/A	11-12 13-14 15-16
5	RS-485 RTS ENABLE with Echo-Back	3-4, 6-8	13-14	N/A	11-12 13-14 15-16
6	RS-485 AUTO ENABLE	3-5, 7-8 (One node must use TX/RX 300 Termination)	13-14	N/A	11-12 13-14 15-16
7	RS-485 AUTO ENABLE with Echo-Back	3-5, 6-8 (One node must use TX/RX 300 Termination)	N/A	N/A	11-12 13-14 15-16

COM2

Mode #	Description	J24	Termination J24		
			TX (100)	RX (100)	TX/RX (300)
1	RS-232	1-2	N/A	N/A	N/A
2	RS-422 RTS ENABLE	3-4 9-10	13-14	17-18	11-12 13-14 15-16
3	RS-422 AUTO ENABLE	3-5, 9-10 (One node must use TX-RX 300 Termination)	N/A	17-18	11-12 13-14 15-16
4	RS-485 RTS ENABLE	3-4, 7-8	13-14	N/A	11-12 13-14 15-16
5	RS-485 RTS ENABLE with Echo-Back	3-4, 6-8	13-14	N/A	11-12 13-14 15-16
6	RS-485 AUTO ENABLE	3-5, 7-8 (One node must use TX/RX 300 Termination)	13-14	N/A	11-12 13-14 15-16
7	RS-485 AUTO ENABLE with Echo-Back	3-5, 6-8 (One node must use TX/RX 300 Termination)	N/A	N/A	11-12 13-14 15-16

Serial Connector Summary (DB9 Pinout)

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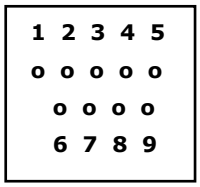


RS-232 Mode	RS-422 Mode	RS-485 Mode
1. DCD	1. N/A	1. N/A
2. RX	2. TX+	2. TX/RX+
3. TX	3. TX-	3. TX/RX-
4. DTR	4. N/A	4. N/A
5. GND	5. GND	5. GND
6. DSR	6. RX+	6. N/A
7. RTS	7. RX-	7. N/A
8. CTS	8. N/A	8. N/A
9. RI	9. N/A	9. N/A

Video Interface

The EPX-855 has an integrated display controller that provides both a CRT and flat panel display interface.

CRT Output Connection

Video output to a standard VGA monitor is made via the connector at **J10**. An adapter cable, part number CBL-234-G-1-1.375, is available from WinSystems to adapt from **J10** to the standard DB15 VGA connector. The pin definitions for the **J10** connector are:

J10

VCC	**14 o o 13**	DDCCLK
GND	**12 o o 11**	DDCDATA
GND	**10 o o 9**	VSYNC
GND	**8 o o 7**	HSYNC
GND	**6 o o 5**	BLUE
GND	**4 o o 3**	GREEN
GND	**2 o o 1**	RED

Flat Panel Connections

WinSystems provides flat panel support with a series of cables and support hardware. Contact your WinSystems' Applications Engineer for the most current list of supported panels. **This manual does not attempt to provide any information about how to connect to specific LCDs**. Attempted connection to any flat panel not directly supported by WinSystems is at the user's risk. Extreme care should be exercised to avoid damaging or destroying the panel. For additional information contact your WinSystems' Applications Engineer.

HAZARD WARNING: LCD panels can require a high voltage for the panel backlight. This high-frequency voltage can exceed 1000 volts and can present a shock hazard. Care should be taken when wiring and handling the inverter output. To avoid the danger of shock and to avoid the panel, make all connection changes with the power removed.

Panel Backlight Connection – Panel backlight connection is made via the connector at **J3**. The pinout for **J3** is shown here for reference.

J3

1	2	3	4
+5V	BACKLIGHT CTRL	GND	+12V

Backlight Enable

J5

4 o o 3
2 o o 1

Avoid Simultaneous Jumpering
Misjumpering could cause damage to the board and/or the Backlight Panel.

(Only One Jumper Selection)

3-4 = Active High Backlight Enable

1-2 = Active Low Backlight Enable

LVDS Connector

There is a dual Low Voltage Differential Signal (LVDS) channel interface available on the EPX-855. Connection is made via the connectors at **J7** and **J6**. The two LVDS connectors at **J7** and **J6** provide a single video interface. **J7** is used for lower resolution panels and high resolution displays may require both connectors.

Visual Index

J7

LV_VDD	1 o o 2	GND
A0-	3 o o 4	A0+
A1-	5 o o 6	A1+
LV_VDD	7 o o 8	GND
A2-	9 o o 10	A2+
A3-	11 o o 12	A3+
LV_VDD	13 o o 14	GND
ACLK-	15 o o 16	ACLK+
DDC_CLK	17 o o 18	GND
DDC_DAT	19 o o 20	GND

J6

LV_VDD	1 o o 2	GND
B0-	3 o o 4	B0+
B1-	5 o o 6	B1+
LV_VDD	7 o o 8	GND
B2-	9 o o 10	B2+
B3-	11 o o 12	B3+
LV_VDD	13 o o 14	GND
BCLK-	15 o o 16	BCLK+
DDC_CLK	17 o o 18	GND
DDC_DAT	19 o o 20	GND

Flat Panel Power

Panel power is +3.3V or +5V and is made by jumpering field **J2**.

Visual Index

J2

4 o o 3
2 o o 1

(Only One Jumper Selection)

1-2 = +3.3V

3-4 = +5V

Avoid Simultaneous Jumpering
Misjumpering could cause damage to the board and/or the Flat Panel.

Fan Connection is made by using jumper field **J1.**

J1

o	o	o
1	2	3
GND	VCC	TACH

Ethernet Controller

The EPX-855 is equipped with two ethernet channels. One is 10/100 and the other provides a Gigabit Ethernet interface.

82562ET 10/100 Mbps (PLC) Ethernet Controller

The Intel 82562ET LAN Ethernet controller is compliant with IEEE 802.3 10Base-T and 100Base-T standards. It has a low power 3.3V CMOS design and supports auto-negotiation. Connection for the 10/100 Mbps Ethernet controller is made via the connector at **J21**. See the Multi-I/O section of this document for more information.

On-board Ethernet activity signals are also provided at **J21**. The Ethernet activity signals are active low. The table below provides more information on LED Activity.

LED ACTIVITY (10/100 Ethernet Controller)

LED8	GREEN	SPEED
LED7	GREEN	ACTIVITY
LED6	GREEN	LINK INTEGRITY

82541ER 10/100/1000 Mbps Gigabit Ethernet Controller

The Intel 82541 Gigabit Ethernet controller chip provides a standard IEEE 802.3 Ethernet interface for 1000Base-T, 100Base_TX and 10Base-T applications (802.3, 802.3u, and 802.3ab). The controller is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps. This PCI 2.3 compliant interface is capable of operating at 33 MHz.

The 82541ER architecture is designed for high performance and efficient power usage. A large 64 KB on-chip packet buffer maintains superior performance.

The RJ-45 connection is available at **J25**.

On-board Ethernet activity signals are also provided. The Ethernet activity signals are active low and are listed below.

LED ACTIVITY (Gigabit Ethernet Controller)

LED2	GREEN	LINK
LED5	GREEN	ACTIVITY
LED4	GREEN	SPEED 10/100
LED3	GREEN	SPEED 1000

USB

The EPX-855 provides four USB 2.0 channels. These are terminated to two 8-pin, 2 mm connectors at **J13** and **J14**. An adapter cable, CBL-275-G-2-0.667, is available from WinSystems for connection. The pinout for the connectors are:

J13, J14

USBGND	**8 o o 7**	USBGND
D1+	**6 o o 5**	D0+
D1-	**4 o o 3**	D0-
USBVCC	**2 o o 1**	USBVCC

NOTE:
Turning on multiple USB devices at the same time can cause the power supply voltage to drop if the power supply does not have enough capacity.

Audio Interface

The EPX-855 has an audio interface designed to provide high-quality audio reproduction for embedded systems use. The EPX-855 provides three stereo line level channels (or 5.1 surround), line level input and microphone.

Audio External Connection

J12 provides connection to line and microphone inputs. WinSystems offers two cables: CBL-270-G-2-1.5 and CBL-270-G-3-1.5 to simplify this connection. The CBL-270-G-3-1.5 cable is a lower cost cable with fewer lines (Line In, Line Out, Microphone Channels). The pin definitions for **J12** are provided below:

J12

ADGND	**18 o o 17**	ADGND
LINE_L	**16 o o 15**	LFE
LINE_R	**14 o o 13**	CENTER
ADGND	**12 o o 11**	ADGND
MIC2_FRONT-L	**10 o o 9**	SUR-L
MIC2-FRONT-R	**8 o o 7**	SUR-R
ADGND	**6 o o 5**	ADGND
MIC1-REAR-L	**4 o o 3**	OUT-L
MIC1-REAR-R	**2 o o 1**	OUT-R

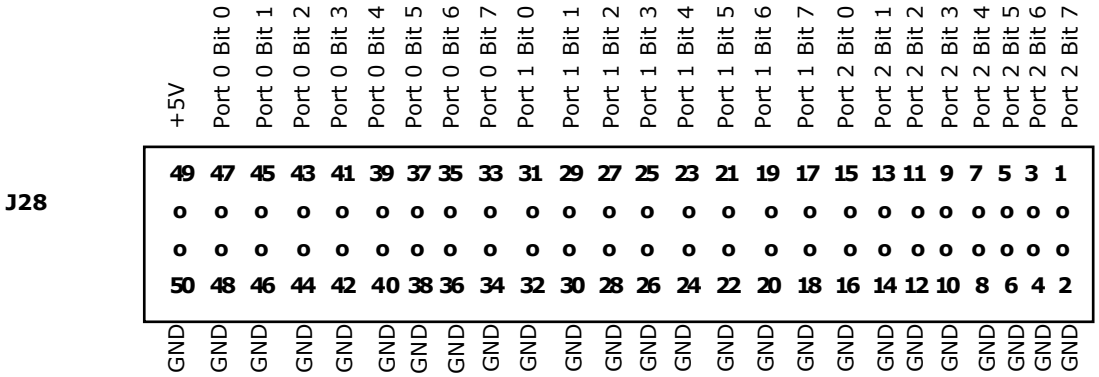
A small PC speaker at **BZ1** is also available. It works separately from the more advanced audio interface. The **BZ1** speaker is intended for simple audio tones.

Digital I/O

The EPX-855 utilizes the WinSystems WS16C48 ASIC high-density I/O chip mapped at a base address of 120H. These 24 lines are capable of fully latched event sensing with sense polarity being software programmable. A 50-pin connector allows for easy mating with industry standard I/O racks. DIO Interrupt selections can be made via the **J16** IRQ jumper. Specific jumpering selections can be found below. For more information on programming the software, refer to the WS16C48 Programming Reference section of this manual.

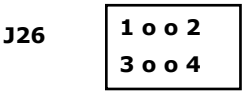
Digital I/O Connectors

The 24 lines of digital I/O are terminated through the 50-pin connectors at **J28**. The pin definitions for **J28** is shown below. All lines have a 10K pull up and power up as high inputs.



Digital I/O VCC Enable

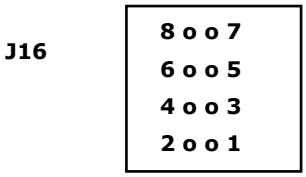
The I/O connectors can provide +5V to an I/O rack or for miscellaneous purposes by jumpering **J20**. When **J20** is jumpered (1-2), +5V is provided at pin 49 of **J28**. It is the user's responsibility to limit current to a safe value (less than 400 mA) to avoid damaging the CPU board.



1-2 +5V is provided at pin 49 of **J28**

3 4 DIO enabled (OPEN)

3-4 DIO disabled



DIO Interrupt Selection (only one selection)

7-8	IRQ 5
5-6	IRQ 10 (default)
3-4	IRQ 15
1-2	none

MiniPCI/802.11 Wireless Support

The EPX-855 includes a MiniPCI socket (**CN1**), located on the back of the board, as another means to add functionality. Though the socket can support other devices, it is most often used to add wireless Ethernet cards from Intel®, Broadcom®, Foxconn® (Atheros), or others.

MiniPCI Device Interface (CN1)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	N/C	2	N/C	63	3.3V	64	FRAME#
	KEY		KEY	65	CLKRUN#	66	TRDY#
3	N/C	4	N/C	67	SERR#	68	STOP#
5	N/C	6	N/C	69	GROUND	70	3.3V
7	N/C	8	N/C	71	PERR#	72	DEVSEL#
9	N/C	10	N/C	73	C/BE(1)#	74	GROUND
11	N/C	12	N/C	75	AD(14)	76	AD(15)
13	N/C	14	N/C	77	GROUND	78	AD(13)
15	N/C	16	RESERVED	79	AD(12)	80	AD(11)
17	INTB#	18	5V	81	AD(10)	82	GROUND
19	3.3V	20	INTA#	83	GROUND	84	AD(09)
21	RESERVED	22	RESERVED	85	AD(08)	86	C/BE(0)#
23	GROUND	24	3.3V AUX	87	AD(07)	88	3.3V
25	CLK	26	RST#	89	3.3V	90	AD(06)
27	GROUND	28	3.3V	91	AD(05)	92	AD(04)
29	REQ#	30	GNT#	93	RESERVED	94	AD(02)
31	3.3V	32	GROUND	95	AD(03)	96	AD(00)
33	AD(31)	34	PME#	97	5V	98	RESERVED_WIP[5]
35	AD(29)	36	RESERVED	99	AD(01)	100	RESERVED_WIP[5]
37	GROUND	38	AD(30)	101	GROUND	102	GROUND
39	AD(27)	40	3.3V	103	N/C	104	M66EN
41	AD(25)	42	AD(28)	105	N/C	106	N/C
43	RESERVED	44	AD(26)	107	N/C	108	N/C
45	C/BE(3)#	46	AD(24)	109	N/C	110	N/C
47	AD(23)	48	IDSEL	111	N/C	112	RESERVED_WIP5
49	GROUND	50	GROUND	113	N/C	114	GROUND
51	AD(21)	52	AD(22)	115	N/C	116	N/C
53	AD(19)	54	AD(20)	117	N/C	118	N/C
55	GROUND	56	PAR	119	N/C	120	N/C
57	AD(17)	58	AD(18)	121	RESERVED	122	N/C
59	C/BE(2)#	60	AD(16)	123	N/C	124	3.3V AUX
61	IRDY#	62	GROUND				

Line Printer Port

The LPT port is a multimode parallel printer port that supports the Standard Bidirectional Parallel Port (SPP), Enhanced Parallel Port (EPP) or Extended Capabilities Port (ECP). The output drivers support 14 mA per line.

Interface is provided at the Multi-I/O connector, **J21,** which is an 80-pin high density connector. WinSystems offers the cable CBL-251-G-2-1.0 to simplify the connection. The default base address for the LPT port is 378.

If a printer is not required, the printer port can also be used as two additional general-purpose I/O ports. The first port is configured as eight input or output only lines. The other port is configured as five input and three output lines.

Keyboard

An integrated 80C42 equivalent keyboard controller supports a PS/2 keyboard. Interface is provided at connector **J21**, which is an 80-pin high density connector. WinSystems offers the cable CBL-251-G-2-1.0 to simplify the connection. The pinout for the connector and cable is detailed in the cable drawing. Optionally, a USB keyboard can be connected in addition to, or instead of the standard PS/2 keyboard.

Mouse Interface

A PS/2 mouse may be attached via the 80-pin high density connector at **J21**. An adapter cable, CBL-251-G-2-1.0, is available from WinSystems to adapt to a conventional PS/2 mouse connector. Optionally, a USB mouse can be connected in addition to, or instead of the standard PS/2 mouse. For more information on the **J21** connector, see the Multi-I/O section of this manual.

Watchdog Timer

The EPX-855 features an advanced watchdog timer which can be used to guard against software lockups. Configuring the Watchdog timer setting in the BIOS CMOS means the watchdog timer can be enabled by the BIOS to start running at power-on. If having the watchdog enabled at power-on is not desired, then it can be enabled after the system has booted using the configuration registers.

Setting a value other than **Disabled** (default 566h = 00h) in the CMOS setting will serve as the starting timeout value at system boot time. The four boot time options available in the CMOS settings table are: *Disabled*, *3 seconds*, *30 seconds* or *300 seconds*.

Note: It is recommended that the long timeout (300 seconds) be used with the watchdog enabled when trying to boot any operating system.

The watchdog timer is serviced by writing the desired timeout value to I/O port 566h. If the watchdog has not been serviced within the allotted time, the circuit resets the CPU.

When the watchdog is disabled at boot, it can be enabled through the watchdog configuration registers at 565h and 566h. The watchdog is enabled by writing a timeout value other than zero into the I/O address 566h. Writing **00h** to the I/O address 566h will disable the watchdog.

The timeout value can be selected as a unit of seconds or minutes. If port 565h bit 7 equals **0**, the timeout value written into port 566h is in minutes. The timeout value written into port 566h is in seconds if port 565 bit 7 equals **1**. Application control timeout options are 1 second to 256 minutes.

Watchdog Timer Examples

Port Address	Port Bit 7 Value	Port Address	Value	Reset Interval
565H	x	566H	00h	DISABLED
565H	1	566H	03h	3 SECONDS
565H	1	566H	1Eh	30 SECONDS
565H	0	566H	04h	3 MINUTES
565H	0	566H	05h	5 MINUTES

Status LED

A green LED, located at **LED9**, is populated on the board, and can be used for any application specific purpose. The LED can be turned on in software (LED IO address = 0x55e). LED9 is wired to pin A33 for **J21**.

write 0x03 to turn it on
write 0x00 to turn it off
write 0x01 to blink once every second (50% duty)
write 0x02 to blink once every 2 seconds (25% duty)

PC/104 Bus Interface

The PC/104 bus is electrically equivalent to the ISA bus. The standard PC/104 I/O card can be populated on EPX-855's PC/104 bus, located at **J19** and **J15**. The interface does not support hot swap capability. The PC/104 bus connector pin definitions are provided here for reference. Refer to the PC/104 Bus Specification for specific signal and mechanical specifications.

J19

GND	**D0 o o C0**	GND
MEMCS16#	**D1 o o C1**	SBHE#
IOCS16#	**D2 o o C2**	LA23
IRQ10	**D3 o o C3**	LA22
IRQ11	**D4 o o C4**	LA21
IRQ12	**D5 o o C5**	LA20
IRQ15	**D6 o o C6**	LA19
IRQ14	**D7 o o C7**	LA18
DACK0#	**D8 o o C8**	LA17
DRQ0	**D9 o o C9**	MEMR#
DACK5#	**D10 o o C10**	MEMW#
DRQ5	**D11 o o C11**	SD8
DACK6#	**D12 o o C12**	SD9
DRQ6	**D13 o o C13**	SD10
DACK7#	**D14 o o C14**	SD11
DRQ7	**D15 o o C15**	SD12
+5V	**D16 o o C16**	SD13
MASTER#	**D17 o o C17**	SD14
GND	**D18 o o C18**	SD15
GND	**D19 o o C19**	KEY

J15

IOCHK#	**A1 o o B1**	GND
SD7	**A2 o o B2**	RESET
SD6	**A3 o o B2**	+5V
SD5	**A4 o o B4**	IRQ9
SD4	**A5 o o B5**	-5V
SD3	**A6 o o B6**	DRQ2
SD2	**A7 o o B7**	-12V
SD1	**A8 o o B8**	SRDY#
SD0	**A9 o o B9**	+12V
IOCHRDY	**A10 o o B10**	KEY
AEN	**A11 o o B11**	SMEMW#
SA19	**A12 o o B12**	SMEMR#
SA18	**A13 o o B13**	IOW#
SA17	**A14 o o B14**	IOR#
SA16	**A15 o o B15**	DACK3#
SA15	**A16 o o B16**	DRQ3
SA14	**A17 o o B17**	DACK1#
SA13	**A18 o o B18**	DRQ1
SA12	**A19 o o B19**	REFRESH#
SA11	**A20 o o B20**	BCLK
SA10	**A21 o o B21**	IRQ7
SA9	**A22 o o B22**	IRQ6
SA8	**A23 o o B23**	IRQ5
SA7	**A24 o o B24**	IRQ4
SA6	**A25 o o B25**	IRQ3
SA5	**A26 o o B26**	DACK2#
SA4	**A27 o o B27**	TC
SA3	**A28 o o B28**	BALE
SA2	**A29 o o B29**	+5V
SA1	**A30 o o B30**	OSC
SA0	**A31 o o B31**	GND
GND	**A32 o o B32**	GND

= Active Low Signal

NOTES:
1. Rows C and D are not required on 8-bit modules.
2. B10 and C19 are key locations. WinSystems uses key pins as connections to GND.
3. Signal timing and function are as specified in ISA specification.
4. Signal source/sink current differ from ISA values.
5. 16 bit bus transfers are performed as 2 8-bit transfers (High byte / Low byte).

PC/104-*Plus* Bus Interface

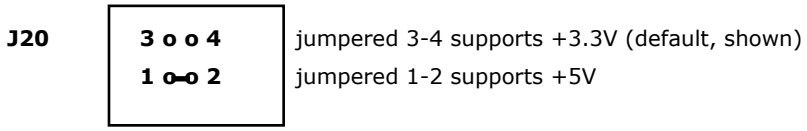
The PC/104-*Plus* is electrically equivalent to the 33 MHz PCI bus and is terminated to a 120-pin, nonstackthrough connector. The standard PC/104-*Plus* I/O modules can be populated on EPX-855's PC/104-*Plus* bus. The interface does not support hot swap capability. The PC/104-*Plus* bus connector is located at **J18**. Refer to the PC/104-*Plus* Bus Specification for specific signal and mechanical specifications. The pin definitions are:

Pin	A	B	C	D
1	GND	RESERVED	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	RESERVED	PAR
10	GND	PERR#	+3.3V	RESERVED
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O
24	GND	REQ2#	+5V	GNT0#
25	GNT1#	VI/O	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD#	+5V	RST#
29	+12V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND

Note: 1. The shaded area denotes power or ground signals.

PC/104-*Plus* VIO Voltage

PC/104-*Plus* VIO Voltage is selected by jumpering **J20**.



WS16C48 Programming Reference

Introduction

This section provides basic documentation for the included I/O routines. It is intended that the accompanying source code equip the programmer with a basic library of I/O functions for the WS16C48 or can serve as the basis from which application specific code can be derived.

Function Definitions

This section describes each of the functions contained in the driver. Where necessary, short examples will be provided to illustrate usage. Any application making use of any of the driver functions should include the header file UIS48.H, which includes the function prototypes and the needed constant definitions.

Note that all of the functions utilize the concept of *bit_number*. The bit_number is a value from 1 to 48 (1 to 24 for interrupt related functions) that correlates to a specific I/O pin. Bit_number 1 is port 0 bit 0 and continues through to bit_number 48 at port 5 bit 7.

INIT_IO – Initializes I/O, set all ports to input

Syntax

void init_io(unsigned io_address);

Description

This function takes a single argument:

io_address – The I/O address of the WS16C48 chip.

There is no return value. This function initializes all I/O pins for input (sets them high), disables all interrupt settings, and sets the image values.

READ_BIT – Reads an I/O port Pin

Syntax

int read_bit(int bit_number);

Description

This function takes a single argument:

bit_number – a value from 1 to 48 specifying the I/O pin to read from.

This function returns the state of the I/O pin. A **1** is returned if the I/O pin is low and a **0** is returned if the pin is high.

WRITE_BIT – Writes a **1** or **0** to an I/O Pin

Syntax

void write_bit(int bit_number, int value);

Description

This function takes two arguments:

bit_number – a value from 1 to 48 specifying the I/O pin to be acted upon.

value - is ether 1 or 0.

This function allows for writing of a single bit to either a **0** or a **1** as specified by the second argument. There is no return value and other bits in the I/O port are not affected.

SET_BIT – Sets the specified I/O Pin

Syntax

void set_bit(int bit_number);

Description

This function takes a single argument:

bit_number – a value from 1 to 48 specifying the I/O pin to be set.

This function sets the specified I/O port bit. Note that setting a bit results in the I/O pin actually going low. There is no return value and other bits in the same I/O port are unaffected.

CLR_BIT – Clears the specified I/O Pin

Syntax

void clr_bit(int bit_number);

Description

This function takes a single argument:

bit_number – a value from 1 to 48 specifying the I/O pin to clear.

This function clears the specified I/O bit. Note that clearing the I/O bit results in the actual I/O pin going high. This function does not affect any bits other than the one specified.

ENAB_BIT – Enables Edge Interrupt, Select Polarity

Syntax

void enab_bit(int bit_number, int polarity);

Description

This function takes two arguments:

bit_number – a value from 1 to 24, specifying the appropriate bit.

polarity - specifies rising or falling edge polarity detect. The constraints RISING and FALLING are defined UIO48.H.

This function enables the edge detection circuitry for the specified bit at the specified polarity. It does not unmask the interrupt controller, install vectors, or handle interrupts when they occur. There is no return value and only the specified bit is affected.

DISAB_INT – Disables Edge Detect Interrupt Detection

Syntax

void disab_int(int bit_number);

Description

This function takes a single argument:

bit_number – a value from 1 to 24 specifying the appropriate bit.

This function shuts down the edge detection interrupts for the specified bit. There is no return value and no harm is done by calling this function for a bit which did not have edge detection interrupts enabled. There is no effect on any other bits.

CLR_INT – Clears the specified pending interrupt

Syntax

void clr_int(int bit_number);

Description

This function takes a single argument:

bit_number – a value from 1 to 24 specifying the bit number to reset the interrupt.

This function clears a pending interrupt on the specified bit. It does this by disabling and reenabling the interrupt. The net result after the call is that the interrupt is no longer pending and is renamed for the next transition of the same polarity. Calling this function on a bit that has not been enabled for interrupts will result in its interrupt being enabled with an undefined polarity. Calling this function with no interrupt pending will have no adverse effect. Only the specified bit is affected.

GET_INT – Retrieves bit number of pending interrupt

Syntax

void get_int(void);

Description

This function requires no arguments.

This function returns either a **0** for no bit interrupts pending or a value between 1 and 24 representing a bit number that has a pending edge detect interrupt. The function returns with the first interrupt found and begins its search at Port 0 bit 0 proceeding through to Port 2 Bit 7. It is necessary to use either clr_int() or disab_int() to avoid returning the same bit continuously. This function may be used in an application's ISE or can be used in the foreground to poll for bit transitions.

Sample Programs

There are three sample programs in source code form included on the EBC-C3PLUS diskette in the UIO48 directory. These programs are not useful by themselves but are provided to illustrate the usage of the I/O functions provided in UIO48.C.

FLASH.C

This program was compiled with Borland C/C++ version 3.1 on the command line with:
bcc flash.c uio48.c

This program illustrates the most basic usage of the WS16C48. It uses three functions from the driver code. The io_init() function is used to initialize the I/O functions and the set_bit() and clr_bit() functions are used to sequence through all 48 bits turning each on and then off in turn.

POLL.C

This program was compiled with Borland C/C++ version 3.1 on the command line with:
bcc poll.c uio48.c

This program illustrates additional features of thw WS16C48 and the I/O library functions. It programs the first 24 bits for input, arms them for falling edge detection, and then polls using the library routine get_init() to determine if any transitions have taken place.

INT.C

This program was compiled with Borland C/C++ version 3.1 on the command line with:
bcc int.c uio48.c

This program is identical in function to the POLL.C program except that interrupts are active and all updating of the transition counters is completed in the background during the interrupt service routine.

Summary

Links to the source code for all three programs as well as the I/O routines can be found on the WinSystems website located at http://www.winsystems.com. These I/O routines along with the sample program should provide for a good basis on which to build an application using the features of the WS16C48.

Cables

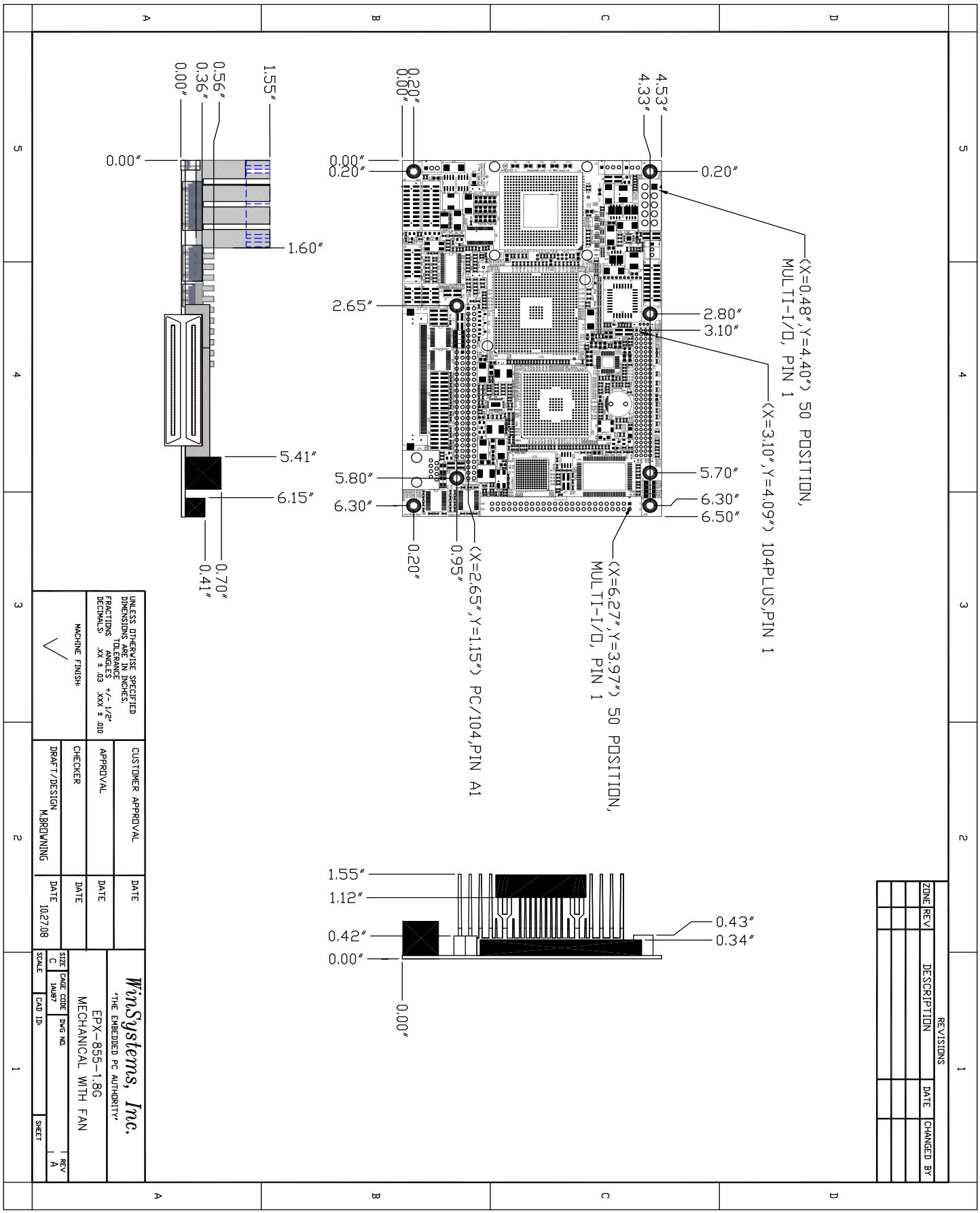
Part Number	Description
CBL-115-4	4-ft., Opto rack interface
CBL-219-G-3-1.5	3-pin to unterminated end 18-in. (Reset)
CBL-270-G-2-1.5	5.1 Audio Access Cable
CBL-SET-347-G-1	Various cables for EPX-855 includes:
CBL-234-G-1-1.375	14-pin ribbon to 15-pin D-sub CRT adapter
CBL-251-G-1-1.5	Multi-I/O Cable
CBL-252-G-1-1.5	1-ft., Multi-Disk Cable
CBL-265-G-2-1.5	Unterminated Power Cable
CBL-270-G-3-1.5	Stereo Audio Access Cable
CBL-275-G-2-0.667	USB Cable
BAT-LTC-E-36-16-1	External 3.6V, 1600 mAH battery with plug-in connector

Software Drivers & Examples

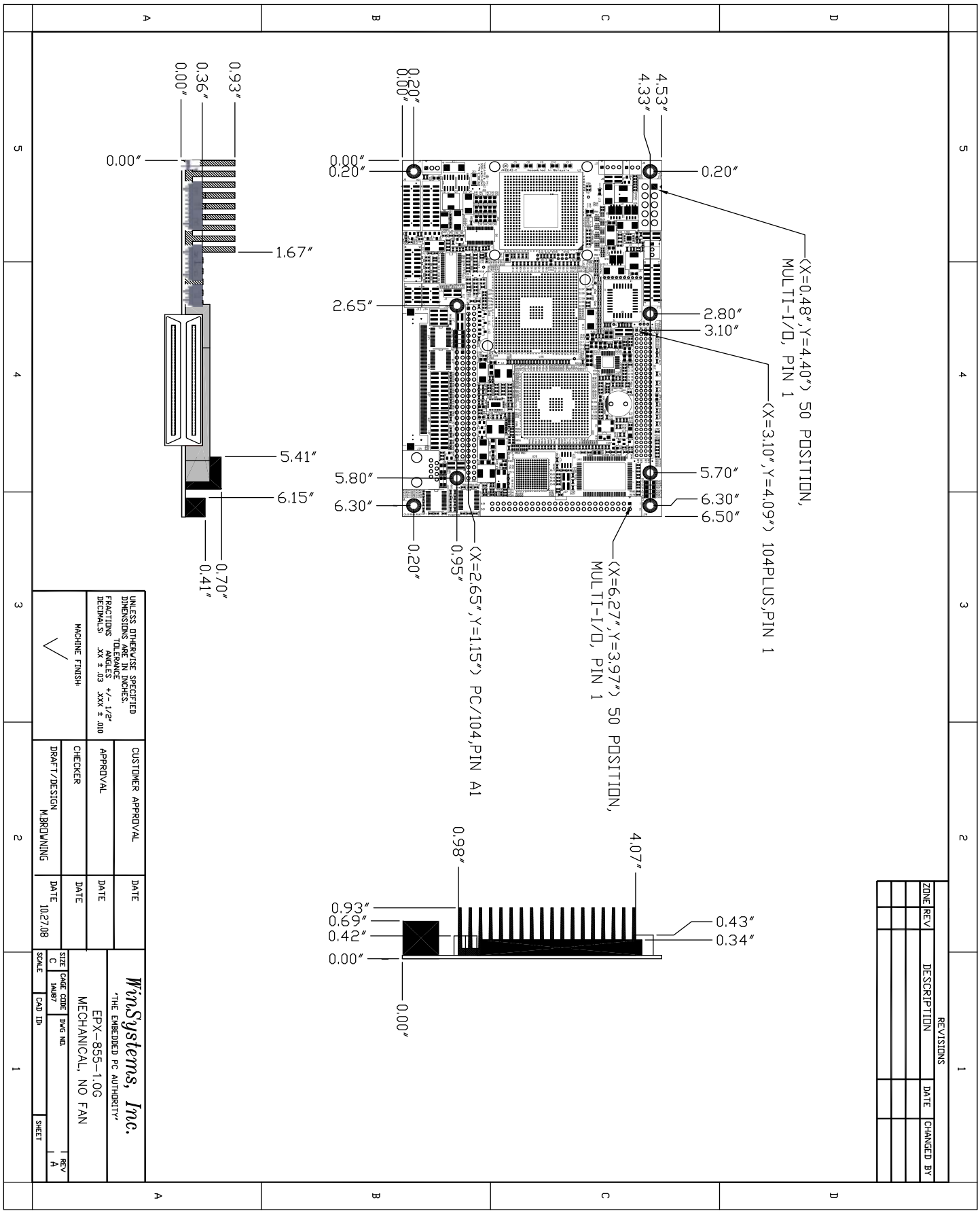
Video Driver	
Windows 2000/XP	win2k_xp141950.exe
Windows 9x	win9x1361.exe
Windows NT4	winnt41361.exe
Linux	i915Graphics.tar.gz
Linux list available at http://www.intelllinuxgraphics.org	
Audio Driver	
Windows 2000/XP	Audio_Drivers.zip
Ethernet Driver	
(Drivers for 82551Q/82559 10/100 Ethernet Controller)	
Windows 2000 and XP Network Adapter Base Drivers	pro2kxpm.zip
Windows NT 4.0 Network Adapter Driver Set	pront4.zip
Windows 98 SE/Me Network Adapter Base Drivers	pro98mem.zip
Windows 95 Driver Release	pro95.zip
MS-DOS and OS/2 Drivers	prodos.zip
NetWare Drivers for PRO Network Adapters	pronware.zip
Linux 2.2 10/100 Adapter Base Driver	e100-2.1.15.tar.gz
Linux 2.4, 2.6 10/100 Adapter Base Driver	e100-3.5.14.tar.gz
DOS Packet Drivers	packet.zip
Gigabit Ethernet Driver	
(From Intel.com)	
Windows 2000/XP Network Adapter Base Drivers	e1000win.zip
Windows XP Embedded Driver	e1000exp.zip
Windows NT 4.0 Network Adapter Driver Set	e1000ndis4.zip
Linux 2.4 10/100/1000 Adapter Base Driver	e1000-5.6.10.1.tar.gz
Utility Program	erutility.zip
Examples	
(For WS16C48 Digital I/O Chip)	
DOS Driver - C Functions	uio48ebc.zip
Linux Drivers - Kernel 2.2, 2.4	linux_uio48_96.zip
Linux Drivers - Kernel 2.6	uio48io_kernel_2.6.zip
Windows XP Driver	wsuio48_96xp.zip

Mechanical Drawing

Fan Included

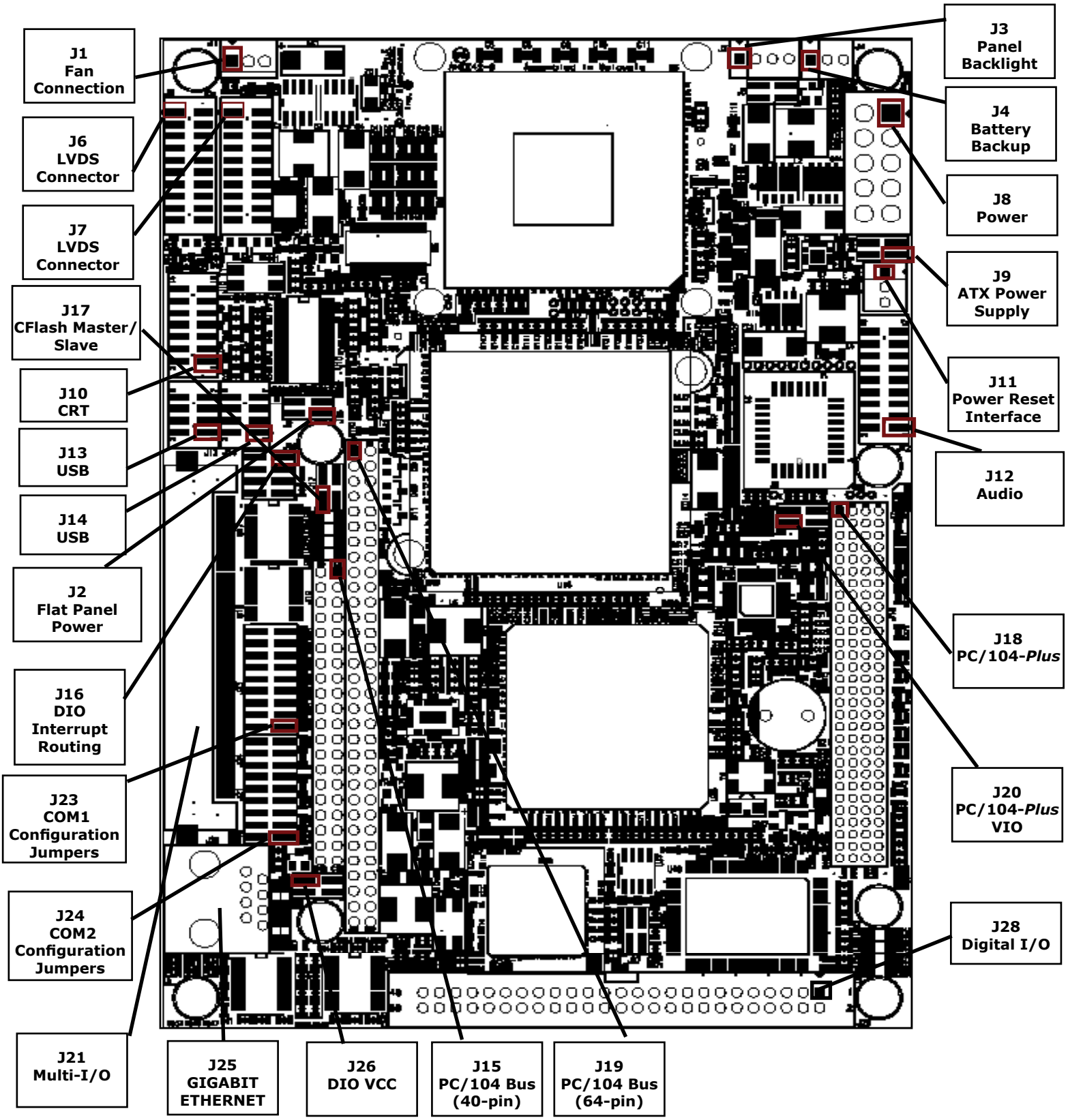


No Fan Included



Jumper Reference

Drawings ONLY - for more detailed information on these parts, refer to the descriptions shown previously in this manual.



NOTE: The reference line to each component part has been drawn to Pin 1, where applicable. Pin 1 is also highlighted with a red square, where applicable.

Power and Reset Interface

J8

+5VSB	**6 o o 1**	PS_ON
+5V	**7 o o 2**	GND
+5V	**8 o o 3**	GND
-12V	**9 o o 4**	+12V
GND	**10 o o 5**	+3.3V*

* - **only connects to the PC/104-*Plus* connector**

Panel Backlight Connection

J3

+5V	BACKLIGHT CTRL	GND	+12V
1	**2**	**3**	**4**
o	**o**	**o**	**o**

Flat Panel Power

J2

4 o o 3
2 o o 1

(Only One Jumper Selection)
1-2 = +3.3V
3-4 = +5V

Avoid Simultaneous Jumpering
Misjumpering could cause damage to the board and/or the Flat Panel.

Power Supply Selection

NOTE: True ATX power supplies are not applicable for embedded systems. They are typically 300W supplies and may not regulate properly with low power embedded systems such as the EPX-855.

J9

4 o o 3
2 o o 1

1-2, 3-4 = AT
1 2, 3 4 = ATX

J11

1 o	RESET
2 o	GND
3 o	PWRBTN

Battery Backup

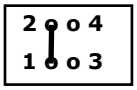
J4

o	**o**	**o**
1	**2**	**3**
GND	+VBAT	NC

(Provides battery backup to RTC and BIOS CMOS.)

CFlash

J17

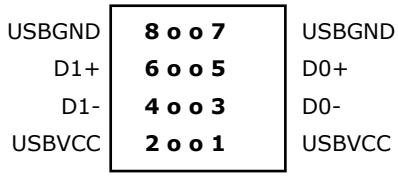


3 4 not used

1-2 CFlash Master, 1 2 CFlash Slave

USB

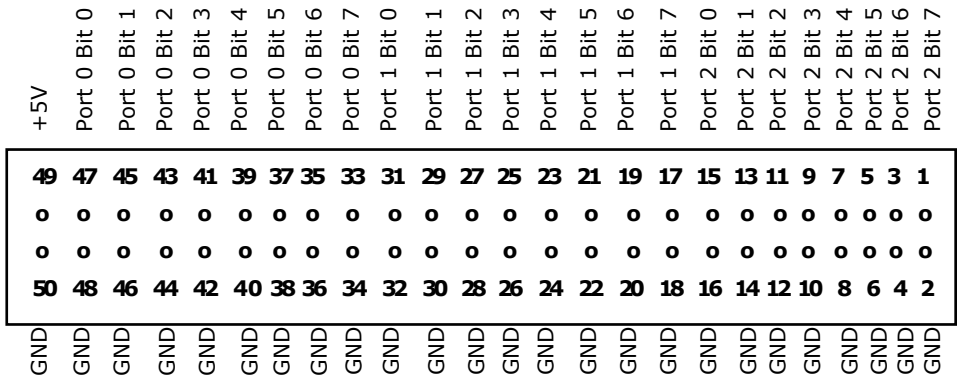
J13, J14



NOTE:
Turning on multiple USB devices at the same time can cause the power supply voltage to drop if the power supply does not have enough capacity.

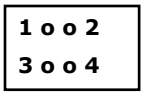
Digital I/O Connectors

J28



Digital I/O VCC Enable

J26

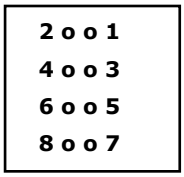


1-2 +5V is provided at pin 49 of **J28**

3 4 DIO enabled (OPEN)

3-4 DIO disabled

J16

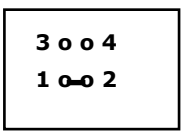


DIO Interrupt Selection (only one selection)

1-2	none
3-4	IRQ 15
5-6	IRQ 10 (default)
7-8	IRQ 5

PC/104-*Plus* VIO Voltage

J20



jumpered 3-4 supports +3.3V (default, shown)

jumpered 1-2 supports +5V

COM1 is configured by setting jumpers at **J23** and COM2 is configured by setting jumpers at **J24**, as shown in the tables below. The tables provide the appropriate jumpering for the various modes.

COM1

Mode #	Description	J23	Termination J23		
			TX (100)	RX (100)	TX/RX (300)
1	RS-232	1-2	N/A	N/A	N/A
2	RS-422 RTS ENABLE	3-4 9-10	13-14	17-18	11-12 13-14 15-16
3	RS-422 AUTO ENABLE	3-5, 9-10 (One node must use TX-RX 300 Termination)	N/A	17-18	11-12 13-14 15-16
4	RS-485 RTS ENABLE	3-4, 7-8	13-14	N/A	11-12 13-14 15-16
5	RS-485 RTS ENABLE with Echo-Back	3-4, 6-8	13-14	N/A	11-12 13-14 15-16
6	RS-485 AUTO ENABLE	3-5, 7-8 (One node must use TX/RX 300 Termination)	13-14	N/A	11-12 13-14 15-16
7	RS-485 AUTO ENABLE with Echo-Back	3-5, 6-8 (One node must use TX/RX 300 Termination)	N/A	N/A	11-12 13-14 15-16

COM2

Mode #	Description	J24	Termination J24		
			TX (100)	RX (100)	TX/RX (300)
1	RS-232	1-2	N/A	N/A	N/A
2	RS-422 RTS ENABLE	3-4 9-10	13-14	17-18	11-12 13-14 15-16
3	RS-422 AUTO ENABLE	3-5, 9-10 (One node must use TX-RX 300 Termination)	N/A	17-18	11-12 13-14 15-16
4	RS-485 RTS ENABLE	3-4, 7-8	13-14	N/A	11-12 13-14 15-16
5	RS-485 RTS ENABLE with Echo-Back	3-4, 6-8	13-14	N/A	11-12 13-14 15-16
6	RS-485 AUTO ENABLE	3-5, 7-8 (One node must use TX/RX 300 Termination)	13-14	N/A	11-12 13-14 15-16
7	RS-485 AUTO ENABLE with Echo-Back	3-5, 6-8 (One node must use TX/RX 300 Termination)	N/A	N/A	11-12 13-14 15-16

Multi-I/O Connector

J21

STROBE (LPT)	**A1 o o B1**	(COM1) DCD
AUTOFD (LPT)	**A2 o o B2**	(COM1) DSR
PD0 (LPT)	**A3 o o B2**	(COM1) RX
ERROR (LPT)	**A4 o o B4**	(COM1) RTS
PD1 (LPT)	**A5 o o B5**	(COM1) TX
INIT (LPT)	**A6 o o B6**	(COM1) CTS
PD2 (LPT)	**A7 o o B7**	(COM1) DTR
SLCTIN (LPT)	**A8 o o B8**	(COM1) RI
PD3 (LPT)	**A9 o o B9**	(COM1) GND
GND (LPT)	**A10 o o B10**	(COM2) DCD
PD4 (LPT)	**A11 o o B11**	(COM2) DSR
GND (LPT)	**A12 o o B12**	(COM2) RX
PD5 (LPT)	**A13 o o B13**	(COM2) RTS
GND (LPT)	**A14 o o B14**	(COM2) TX
PD6 (LPT)	**A15 o o B15**	(COM2) CTS
GND (LPT)	**A16 o o B16**	(COM2) DTR
PD7 (LPT)	**A17 o o B17**	(COM2) RI
GND (LPT)	**A18 o o B18**	(COM2) GND
ACK (LPT)	**A19 o o B19**	(COM3) DCD
GND (LPT)	**A20 o o B20**	(COM3) DSR
BUSY (LPT)	**A21 o o B21**	(COM3) RX
GND (LPT)	**A22 o o B22**	(COM3) RTS
PE (LPT)	**A23 o o B23**	(COM3) TX
GND (LPT)	**A24 o o B24**	(COM3) CTS
SLCT (LPT)	**A25 o o B25**	(COM3) DTR
RX+ (ETH)	**A26 o o B26**	(COM3) RI
RX-(ETH)	**A27 o o B27**	(COM3) GND
TX+ (ETH)	**A28 o o B28**	(COM4) DCD
TX-(ETH)	**A29 o o B29**	(COM4) DSR
LED0 (ETH)	**A30 o o B30**	(COM4) RX
LED1 (ETH)	**A31 o o B31**	(COM4) RTS
LED2 (ETH)	**A32 o o B32**	(COM4) TX
LED3 (ETH)	**A33 o o B33**	(COM4) CTS
+5V	**A34 o o B34**	(COM4) DTR
RESET	**A35 o o B35**	(COM4) RI
GND	**A36 o o B36**	(COM4) GND
MDAT (MOUSE)	**A37 o o B37**	(KYBD) KCLK
GND (MOUSE)+5V	**A38 o o B38**	(KYBD) KDAT
(MOUSE)	**A39 o o B39**	(KYBD) GND
MCLK (MOUSE)	**A40 o o B40**	(KYBD) +5V

Specifications

Electrical

EPX-855 CPU	: 1 GHz Intel ZCD or 1.8 GHz Pentium M
PC/104 Interface	: 16-bit, nonstackthrough
PC/104-*Plus* Interface	: 32-bit PCI, nonstackthrough
Ethernet	: 10/100 Mbps (DA82562ET); 10/100/1000 Mbps (82541)
USB 2.0	: Four (4) ports
Serial Interface	: Four (4) Serial channels with RS-232 levels Two (2) channels with optional RS-422/485
802.11	: Optional MiniPCI card supported
Audio	: AC97 with MIC, SPKR and LINE OUT
LPT Interface	: Bidirectional LPT with ECP/EPP
Digital I/O Interface	: 24 I/O lines, TTL compatible
EIDE interface	: Supports two (2) drives
VCC	: +5V ±5% required, 2.1A typical for Intel® 1.0 GHz ZCD +5V required, 4.25A typical for Intel® 1.8 GHz Pentium M™

System Memory

Addressing	: Up to 1 GB 200-pin SDRAM (accessory available for separate purchase)

Solid State Disk

CompactFlash	: One (1) Type I/II socket

Mechanical

Dimensions	: 4.50” x 6.50” (115 mm x 165 mm)

Connectors

Keyboard	: Standard PS/2 or USB interface
Mouse	: Standard PS/2 or USB interface

Environmental

Operating Temperature	: -40°C to +70°C (1GHz without fan or 1.8GHz with fan) : -40°C to +70°C (1.8GHz with fan) : -40°C to +85°C (1GHz with fan)

Mating Connectors

J21	Multi-I/O	Hirose FX2BA-80SA-1.27
J22	Drives	Hirose FX2BA-80SA-1.27
J10	Video	Molex Housing 51110-1451 Molex Pin 50394-8051
J13	Dual USB	Molex Housing 51110-0851 Molex Pin 50394-8051
J14	Dual USB	Molex Housing 51110-0851 Molex Pin 50394-8051
J12	Audio	Molex Housing 51110-1851 Molex Pin 50394-8052
J6	LVDS	Molex Housing 51110-2051 Molex Pin 50394-8052
J7	LVDS	Molex Housing 51110-2051 Molex Pin 50394-8052
J28	DIO	ITW-Pancon Housing 050-050-455A ITW-Pancon Strain Relief 050-000-050 ITW-PanconPolarizing Key 100-000-043
J15	PC/104 8-bit	Samtec ESQ-132-14-G-D
J19	PC/104 16-bit	Samtec ESQ-120-14-G-D
J18	PC/104-*Plus*	Samtec ESQT-130-02-G-Q-368
J8	Power	Molex Housing 39-01-2105 Molex Pins 39-00-0039
J3	Backlight	Molex Housing 22-01-2047 Molex Pin 08-55-0102
J4	Battery	Molex Housing 22-01-2037 Molex Pin 08-55-0102
J1	Fan	Molex Housing 22-01-2037 Molex Pin 08-55-0102
J11	Power Reset	Molex Housing 22-01-2037 Molex Pin 08-55-0102

WARRANTY REPAIR INFORMATION

WARRANTY
(http://www.winsystems.com/company/warranty.cfm)

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WARRANTY SERVICE

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2. You must send the product postage prepaid and insured. You must enclose the products in an anti-static bag to protect from damage by static electricity. WinSystems is not responsible for damage to the product due to static electricity.