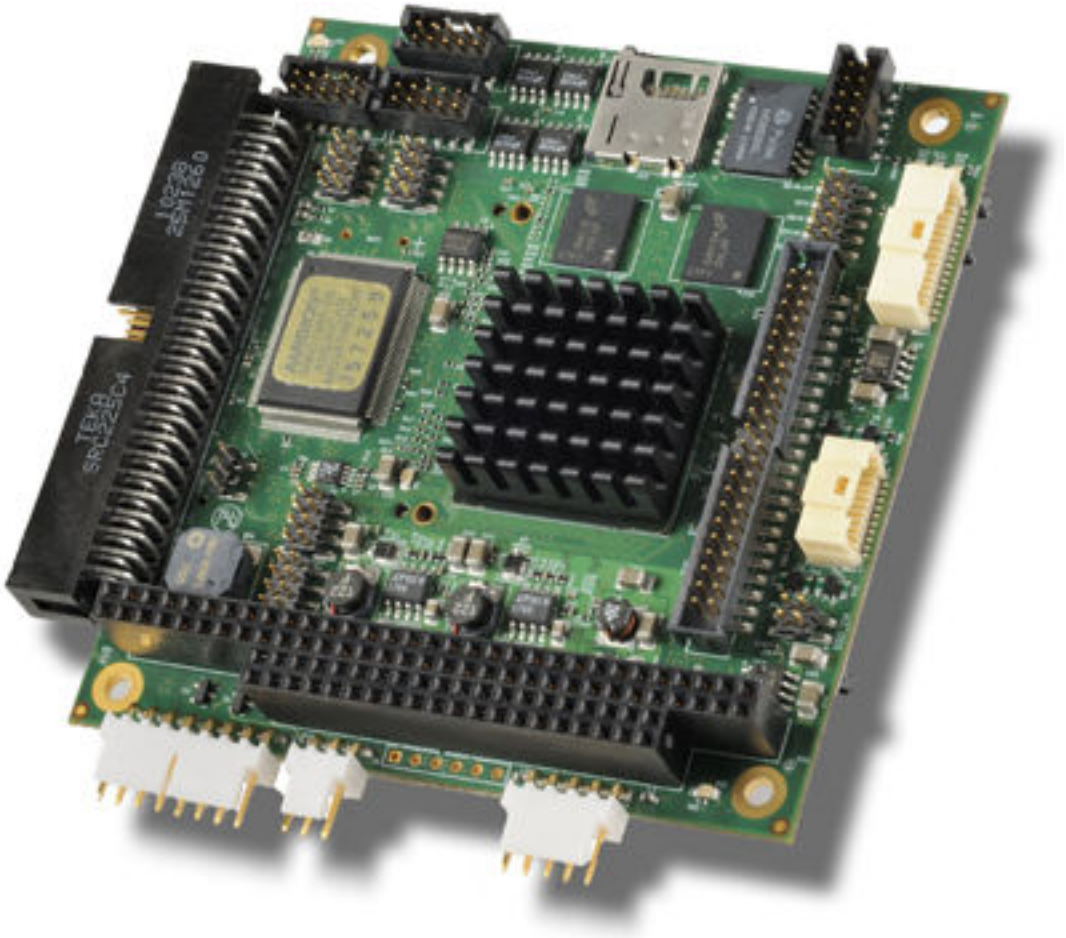
PCM-VDX-2-512

PC/104 Single Board Computer
with Vortex86DX Processor

PRODUCT MANUAL



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MANUAL REVISION HISTORY

P/N 400-0373-000

Revision Date Code	ECO Number
110706	Initial Release
110708	
110725	
110727	
110819	
111117	
120809	
120921	12-107
140418	14-39
140703	
140808	14-74

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BEFORE YOU BEGIN

WinSystems offers best practice recommendations for using and handling WinSystems embedded PCs. These methods include valuable advice to provide an optimal user experience and to prevent damage to yourself and/or the product.

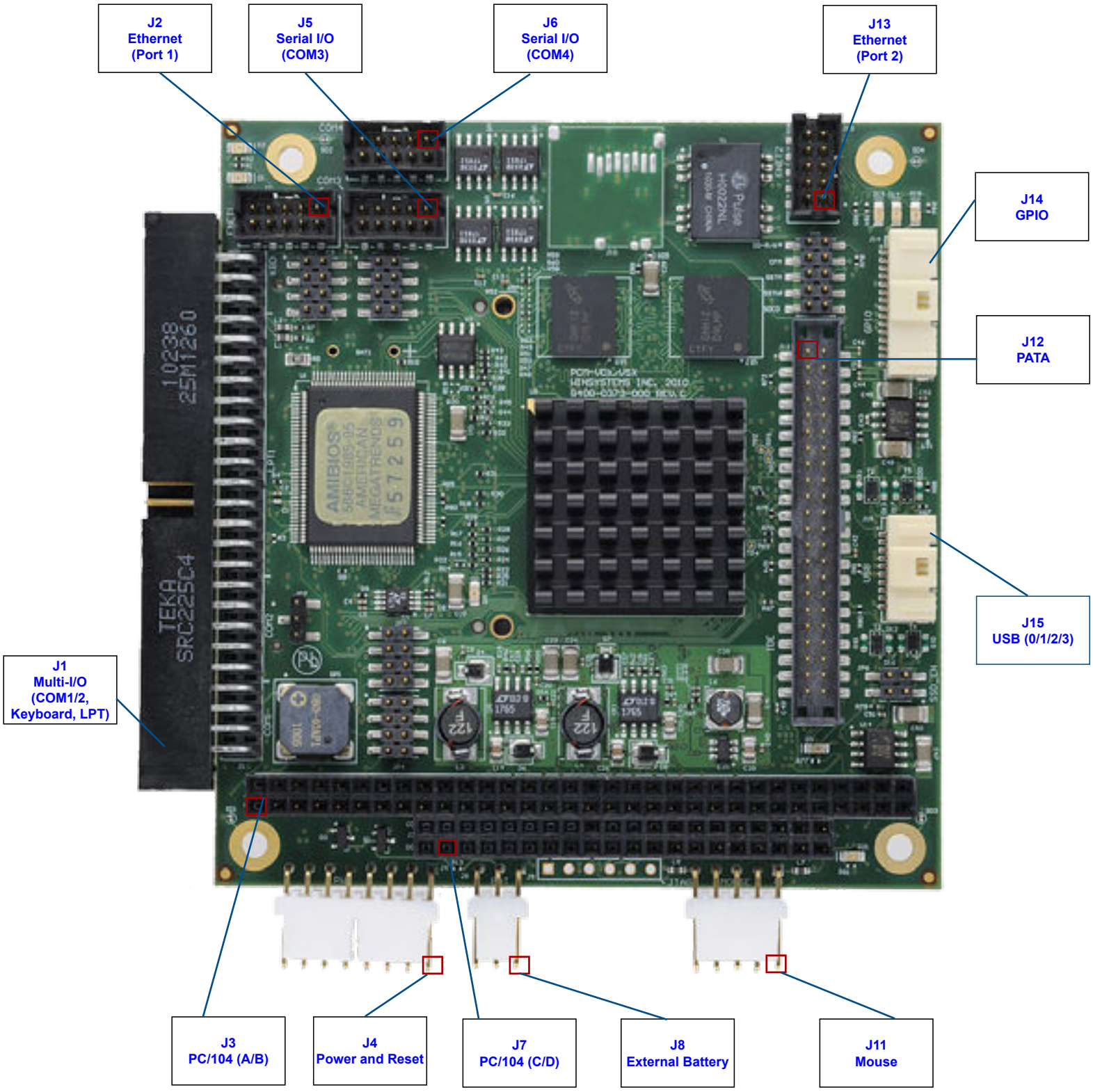
YOU MAY VOID YOUR WARRANTY AND/OR DAMAGE AN EMBEDDED PC BY FAILING TO COMPLY WITH THESE BEST PRACTICES.

Reference **Appendix - A** for **Best Practices**.

Please review these guidelines carefully and follow them to ensure you are successfully using your embedded PC.
This product ships with a heat sink. Product warranty is void if the heat sink is removed from the product.

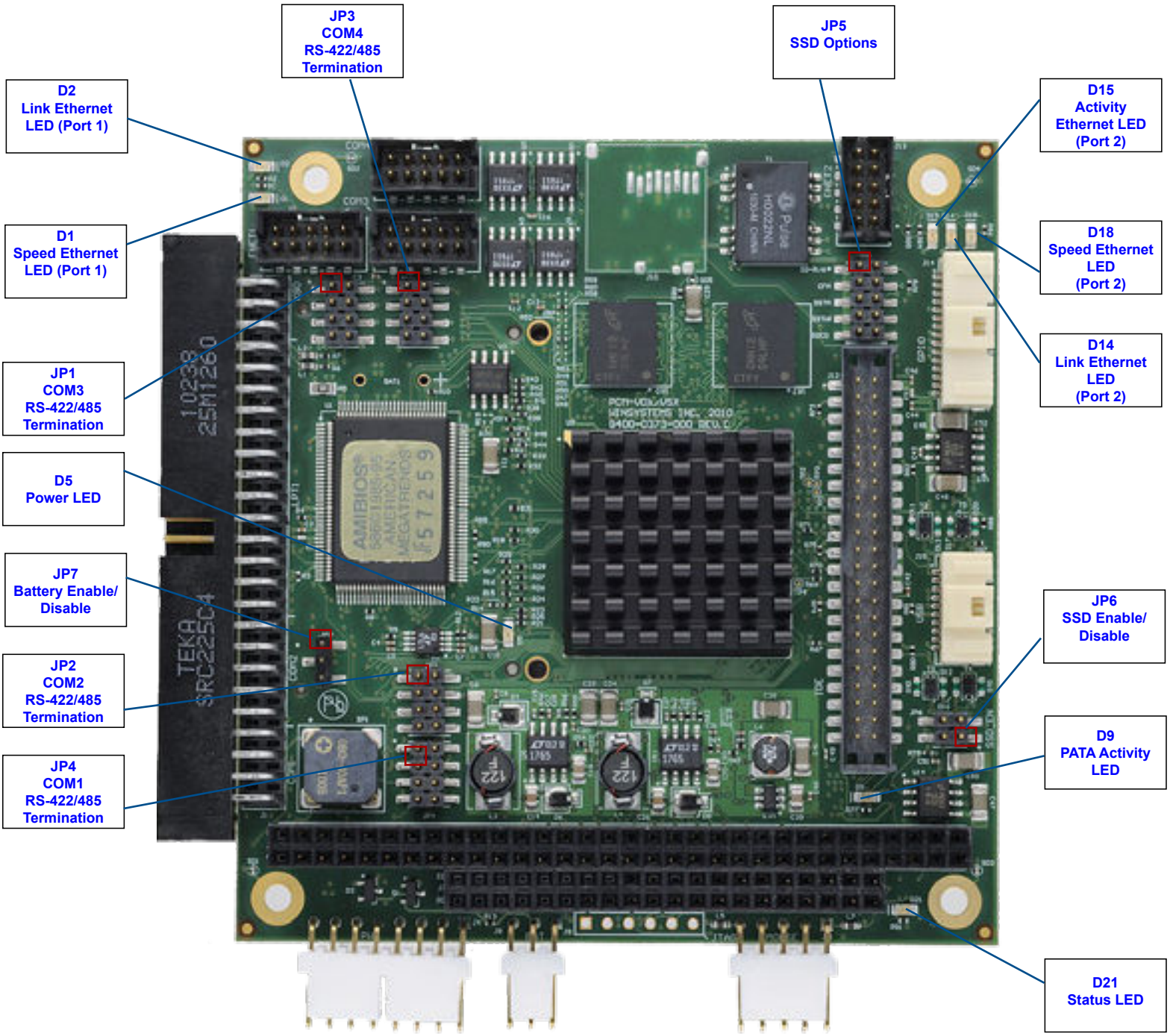
For any questions you may have on WinSystems products, contact our Technical Support Group at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

Visual Index - Top View (Connectors)



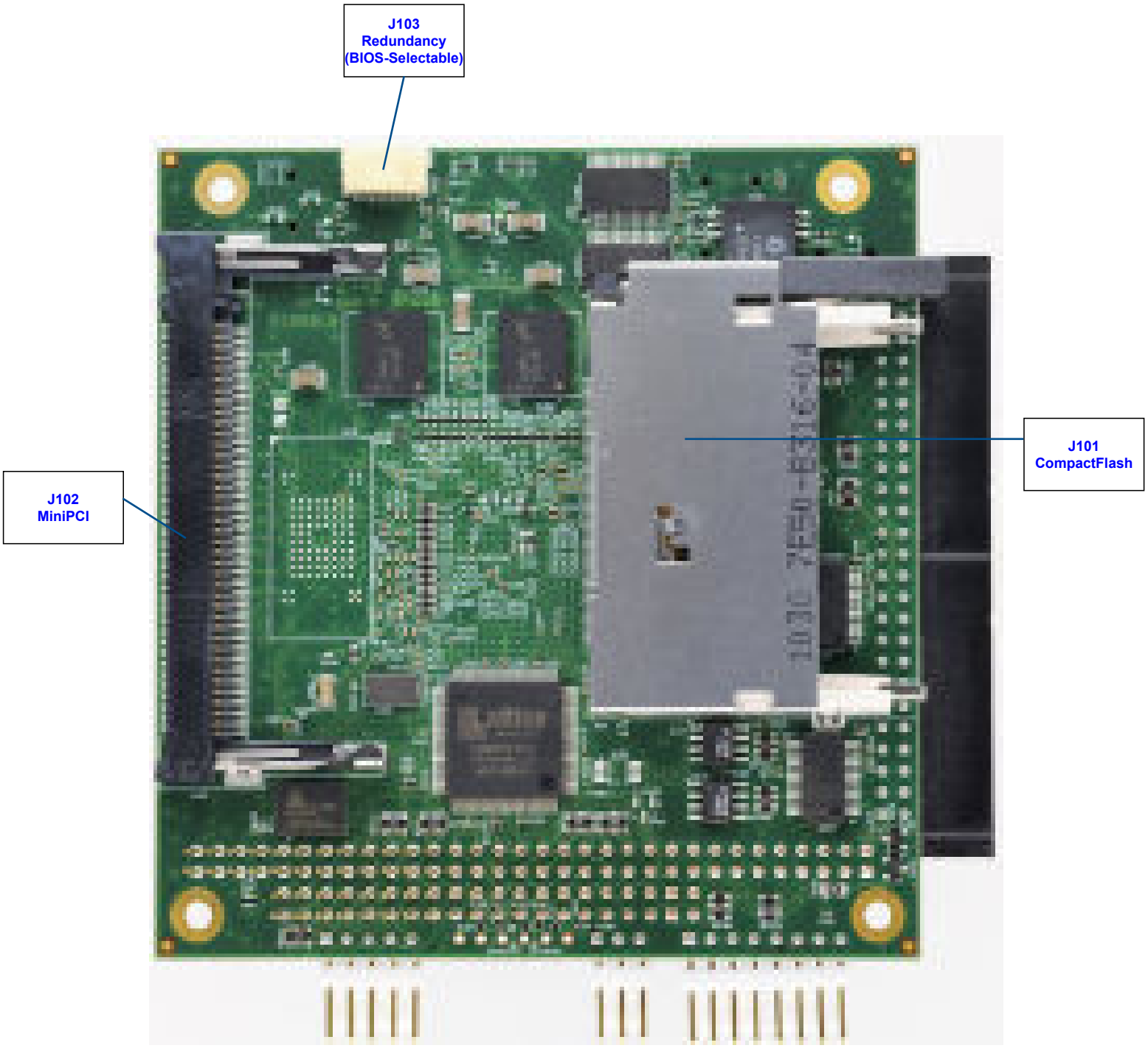
NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

Visual Index - Top View (Jumpers & LEDs)



NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

Visual Index - Bottom View

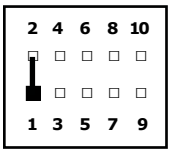


Jumper Reference

NOTE: Jumper Part# SAMTEC 2SN-BK-G is applicable to all jumpers. These are available in a ten piece kit from WinSystems (Part# KIT-JMP-G-200).

JP5 - Solid State Disk Options

JP5



CompactFlash Master (default)	1-2
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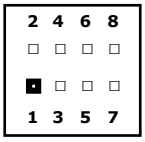
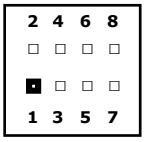
Micro SD Card Write Protect Enable	9-10
Micro SD Card Write Protect Disable	9 10

JP1 - COM3, JP2 - COM2, JP3 - COM4, JP4 - COM1

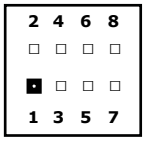
JP1 (COM3)



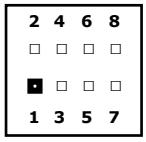
JP2 (COM2)



JP3 (COM4)



JP4 (COM1)



RS-422 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX± pair		7-8
RX (100): Places a 100Ω Resistor across the RX± pair		1-2
TX/RX(300):	Places a 100Ω Resistor from +5V to TX+	5-6
	Places a 100Ω Resistor between TX±	7-8
	Places a 100Ω Resistor from Ground to TX-	3-4

Revision prior to E PCB products require a wire-wrap jumper from 2-3.

Revision prior to E PCB products require a wire-wrap jumper from 1-4.

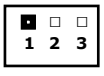
RS-485 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX/RX± pair		7-8
TX/RX(300):	Places a 100Ω Resistor from +5V to TX/RX+	5-6
	Places a 100Ω Resistor between TX/RX±	7-8
	Places a 100Ω Resistor from Ground to TX/RX-	3-4

Revision prior to E products require a wire-wrap jumper from 1-4.

JP7 - On-board Battery (Enable/Disable)

Master Battery Enable

JP7



Enables On-board Battery*	1-2
Enables External Battery (default)	1 2
NC	2-3

***Applicable to OEM models only.**

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

INTRODUCTION

This manual is intended to provide the necessary information regarding configuration and usage of the PCM-VDX-2-512 single board computer. WinSystems maintains a Technical Support Group to help answer questions not adequately addressed in this manual. Contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

FEATURES

CPU
- 1 GHz DMP Vortex (PCM-VDX-2-512)

Compatible Operating Systems
- Linux, DOS, x86 RTOS

Memory
- 1 MB SRAM (Battery-backed user data space)
- 512 MB of DDR2 SDRAM (Soldered)
- 512 MB SSD (Optional on-board Flashdisk)

BIOS
- AMI

Ethernet
- Two 10/100 Mbps (one using Vortex86DX LAN and one using RTL8100C LAN)

Digital I/O
- 16 lines General Purpose Input/Output (GPIO)

Power
- +5V required,1.2A typical

Serial I/O
- 4 serial ports (RS-232/422/485)

USB
- 4 USB 2.0 ports

PATA
- 1 PATA controller

CompactFlash
- Types I & II

Micro SD
- Bootable

Line Printer Port
- ECP/EPP

Watchdog Timer
- Up to 255 minute reset

Bus Expansion
- PC/104
- MiniPCI

Industrial Operating Temperature
- -40°C to 85°C

Form Factor

- 3.60” x 3.80” (90 mm x 96 mm)

Additional Features

- RoHS compliant
- Real-time clock/calendar
- Activity status LEDs on-board
- PS/2 Keyboard and Mouse

System

The PCM-VDX-2-512 is a fanless PC/104 single board computer (SBC) based upon the ultra low power Vortex86DX processor. It requires about 6 Watts under full load while operating over an extended temperature range of -40°C to 85°C. The board has 512 MB soldered on DDR2 SDRAM, Ethernet, USB, serial and parallel I/O, as well as PC/104, MiniPCI expansion, and optional external battery. This board replaces older generation WinSystems’ and other manufacturers’ 386SX, 486DX, 586, and SC520 based SBCs. A 500 MHz model is also available.

Memory

The PCM-VDX-2-512 board is built with 512 MB of SDRAM soldered directly to the PCB. Additionally, 512 MB of soldered-on flash SSD is optional for this board. 1 MB of SRAM is included for user data space. This RAM may be battery backed to maintain data integrity during power off conditions.

FUNCTIONALITY

I/O Port Map

Following is a list of I/O ports used on the PCM-VDX-2-512. I/O addresses marked with a ** are generally unused and should be the first choice in I/O address selection for external I/O boards.

NOTE: The PCM-VDX-2-512 uses a PnP BIOS resource allocation. Care must be taken to avoid contention with resources allocated by the BIOS.

HEX Range	Usage
0000h-000Fh	DMA 8237-1
0010h-0017h	Reserved Redundancy
0018h-001Fh	Free
0020h-0021h	PIC 8259-1
0022h-0023h	6117D configuration port
0024h-002Dh	Free
002Eh-002Fh	Forward to LPC BUS
0030h-003Fh	Free
0040h-0043h	Timer counter 8254
0044h-0047h	Free
0048h-004Bh	PWM counter 8254
004Ch-004Dh	Free
004Eh-004Fh	Forward to LPC Bus
0050h-005Fh	Free
0060h	Keyboard data port
0061h	Port B + NMI control port
0062h-0063h	8051 download 4K address counter
0064h	Keyboard status port
0065h	Watchdog0 reload counter (Vortex internal WD)
0066h	8051 download 8-bit data port
0067h	Watchdog1 reload counter (Vortex internal WD)
0068h-006Dh	Watchdog1 control register (Vortex internal WD)
006Eh-006Fh	Free
0070h-0071h	CMOS RAM port
0072h-0075h	MTBF counter
0076h-0077h	Free
0078h-007Ch	GPIO port 0,1,2,3,4 default setup
007Dh-007Fh	Free
0080h-008Fh	DMA page register
0090h-0091h	Free
0092h	System control register
0093h-0097h	Free
0098h-009Ch	GPIO direction control
00A0h-00A1h	PIC 8259-2
00A2h-00BFh	Free
00C0h-00DFh	DMA 8237-2
00E0h-00FFh	Free
0100h-0101h	GPCS1 default setting address
0102h-016Fh	Free
0170h-0177h	Reserved IDE1
01E8h-01ECh	Reserved
01EDh	Status LED
01EEh-01EFh	Watchdog Timer Control (Legacy)

HEX Range	Usage
01F0h-01EFh	IDE0 (IRQ 14)
1F80h-0219h	Free
0220h-0227h	1 MB SRAM (Battery-backed user data space)
0228h-02AFh	Free
02B0h-02DFh	Video Controllers (typically reserved, video)
02E0h-02E7h	Free
02E8h-02EFh	COM4 (IRQ11) (default)
02F0h-02F7h	Free
02F8h-02FFh	COM2 (IRQ3) (default)
0300h-0375h	Free
0376h	IDE1 ATAPI device control write only register
0378h-037Bh	LPT Default (IRQ7, DM0) (default)
037Ch-03AFh	Free
03B0h-03BBh	Video Controllers (typically reserved, video)
03C0h-03DFh	Video Controllers (typically reserved, video)
03E0h-03E7h	Free
03E8h-03EFh	COM3 (IRQ9) (default)
03F0h-03F7h	Reserved Legacy Floppy
03F6h	IDE0 ATAPI device control write only register
03F8h-03FFh	COM1 (IRQ4) (default)
0480h-048Fh	DMA High page register
0490h-0499h	Instruction counter register
04D0h-04D1h	8259 Edge/level control register
0564h-0568h	Advanced Watchdog
0CF8h-0CFFh	PCI configuration port
D400h-D4FFh	On-board LAN
FC00h-FC05h	SPI Flash BIOS control register
FC08h-FC0Dh	External SPI Bus control register (output pin configurable GPIO3[0-3])

Memory Map

HEX Range	Usage
0000:0000-9000:FFFF	System RAM
A000:0000-A000:FFFF	EGA/VGA Video Memory
B000:0000-B000:7FFF	MDA RAM, Hercules graphics display RAM
B000:8000-B000:FFFF	CGA display RAM
C000:0000-C000:7FFF	EGA/VGA BIOS ROM
C000:8000-C000:FFFF	Boot ROM enable.
D000:0000-D700:FFFF	Expansion ROM space.
D800:0000-DB00:FFFF	SPI FLASH Emulation Floppy A Enable
DC00:0000-DF00:FFFF	Expansion ROM space.
E000:0000-E000:FFFF	USB Legacy SCSI ROM space.
F000:0000-F000:FFFF	Motherboard BIOS

Interrupt Map

Hardware Interrupts (IRQs) are supported for both PC/104 (ISA) and PCIe devices. The user must reserve IRQs in the BIOS CMOS configuration for use by legacy devices. The PCIe/PnP BIOS will use unreserved IRQs when allocating resources during the boot process. The table below lists IRQ resources as used by the PCM-VDX-2-512.

IRQ0	18.2 Hz heartbeat
IRQ1	Keyboard
IRQ2	Chained to Slave controller (IRQ9)
IRQ3	COM2 *
IRQ4	COM1 *
IRQ5	USB/On-board Ethernet
IRQ6	USB
IRQ7	LPT *
IRQ8	Real-Time Clock
IRQ9	COM3 *
IRQ10	Available
IRQ11	COM4 *
IRQ12	Mouse
IRQ13	Floating point processor
IRQ14	IDE
IRQ15	Available

*	These IRQ references are default settings that can be changed by the user in the CMOS Settings utility. Reference the PCI Configurations section under Advanced Settings.
**	IRQ9 is commonly used by ACPI when enabled and may be unavailable (depending on operating system) for other uses.
***	IRQ15 is currently unavailable under the Windows operating systems.
Some IRQs can be freed for other uses if the hardware features they are assigned to are not being used. To free an interrupt, use the CMOS setup screens to disable any unused board features or their IRQ assignments.	

DMA Map

DMA#	Description	Usage
DMA0	Available	
DMA1	Available	
DMA2	Available	
DMA3	Available	
DMA4	Available	
DMA5	Available	
DMA6	Available	
DMA7	Available	

Watchdog Timer

The PCM-VDX-2-512 features an advanced watchdog timer which can be used to guard against software lockups. Two interfaces are provided to the watchdog timer. The Advanced interface is the most flexible and recommended for new designs. The other interface option is provided for software compatibility with older WinSystems single board computers.

Advanced

The watchdog timer can be enabled in the BIOS Settings by entering a value for Watchdog Timeout on the Chipset → SouthBridge Configuration screen. Once the operating system is loaded, the watchdog can be disabled or reconfigured in the application software.

NOTE: It is recommended that a long timeout be used if the watchdog is enabled when trying to boot any operating system.

The watchdog can be enabled, disabled or reset by writing the appropriate values to the configuration registers located at I/O addresses 565h and 566h. The watchdog is enabled by writing a timeout value other than zero to the I/O address 566h and disabled by writing **00h** to this I/O address. The watchdog timer is serviced by writing the desired timeout value to I/O port 566h. If the watchdog has not been serviced within the allotted time, the circuit resets the CPU.

The timeout value can be set from 1 second to 255 minutes. If port 565h bit 7 equals **0**, the timeout value written into I/O address 566h is in minutes. The timeout value written to address 566h is in seconds if port 565 bit 7 equals **1**.

Watchdog Timer Examples

Port Address	Port Bit 7 Value	Port Address	Value	Reset Interval
565H	x	566H	00h	DISABLED
565H	1	566H	03h	3 SECONDS
565H	1	566H	1Eh	30 SECONDS
565H	0	566H	04h	4 MINUTES
565H	0	566H	05h	5 MINUTES

Software watchdog timer PET = PORT 566H, write the timeout value.

Legacy

This interface is provided for legacy software support only and is not recommended for new development.

The watchdog can be enabled or disabled via software by writing an appropriate timeout value to I/O port 1EEH. See the chart provided below.

Port Address	Value	Reset Interval
1EEH	00h	DISABLED
	01h	2 SECONDS
1EFH	ANY	RESET TIMER

Real-Time Clock/Calendar

A real-time clock is used as the AT-compatible clock/calendar. It supports a number of features including periodic and alarm interrupt capabilities. In addition to the time and date keeping functions, the system configuration is kept in CMOS RAM contained within the clock section. A battery must be installed for the real-time clock to retain time and date during a power down.

POWER

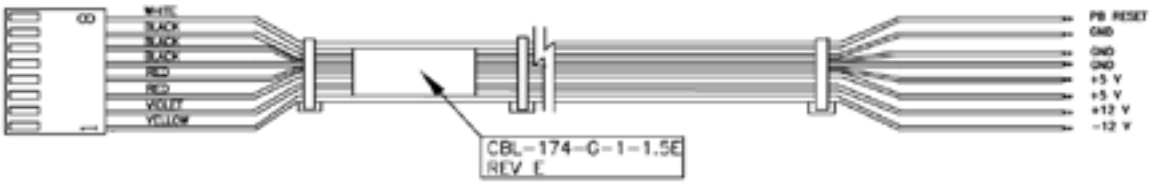
J4 - Power and Reset

Visual Index

PCB Connector: **MOLEX 22-12-2084 (J4)**
Mating Connector: **MOLEX 10-11-2083 (Housing)**
MOLEX 08-55-0124 (Crimp)

J4

1 ■	-12V
2 □	+12V
3 □	+5V
4 □	+5V
5 □	GND
6 □	GND
7 □	GND
8 □	PBRESET



CBL-174-G-1-1.5

Power is applied to the PCM-VDX-2-512 via the connector at **J4**. WinSystems offers the cable **CBL-174-G-1-1.5** to simplify this connection.

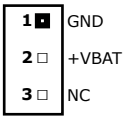
BATTERY BACKUP

J8 - External Battery

Visual Index

PCB Connector: **MOLEX 22-12-2034 (J8)**
Mating Connector: **MOLEX 22-01-3037 (Housing)**
MOLEX 08-55-0102 (Crimp)

J8



(For external battery. Provides battery backup to RTC and BIOS CMOS.)

An optional external battery, connected at **J8**, supplies the PCM-VDX-2-512 board with standby power for the real-time clock and CMOS setup RAM. An extended temperature lithium battery is available from WinSystems, part number BAT-LTC-E-36-16-1 or BAT-LTC-E-36-27-1.

A power supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or standby voltage to the circuits selected for backup. The battery automatically switches ON when the VCC of the systems drops below the battery voltage and back OFF again when VCC returns to normal.

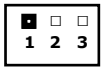
For OEM applications, an on-board battery may be populated. Please contact your WinSystems' Application Engineer for additional information.

JP7 - On-board Battery (Enable/Disable)

Visual Index

Master Battery Enable

JP7



Enables On-board Battery*	1-2
Enables External Battery (default)	1 2
NC	2-3

***Applicable to OEM models only.**

SPEAKER

SP1 - Speaker

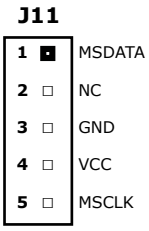
Speaker

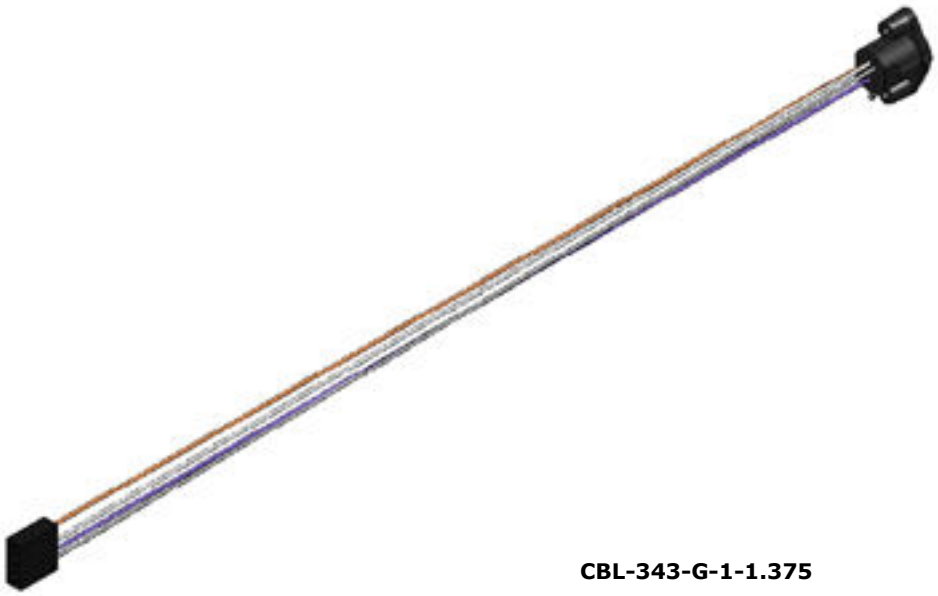
An on-board speaker, **SP1**, is available for sound generation.

J11 - Mouse

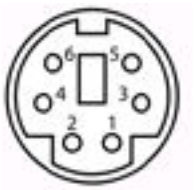
Visual Index

PCB Connector: **MOLEX 22-12-2054 (J11)**
Mating Connector: **MOLEX 08-55-0102 (Crimp)**





CBL-343-G-1-1.375



Pin	Description
1	MSDATA
2	NC
3	GND
4	VCC
5	MSCLK
6	N/C

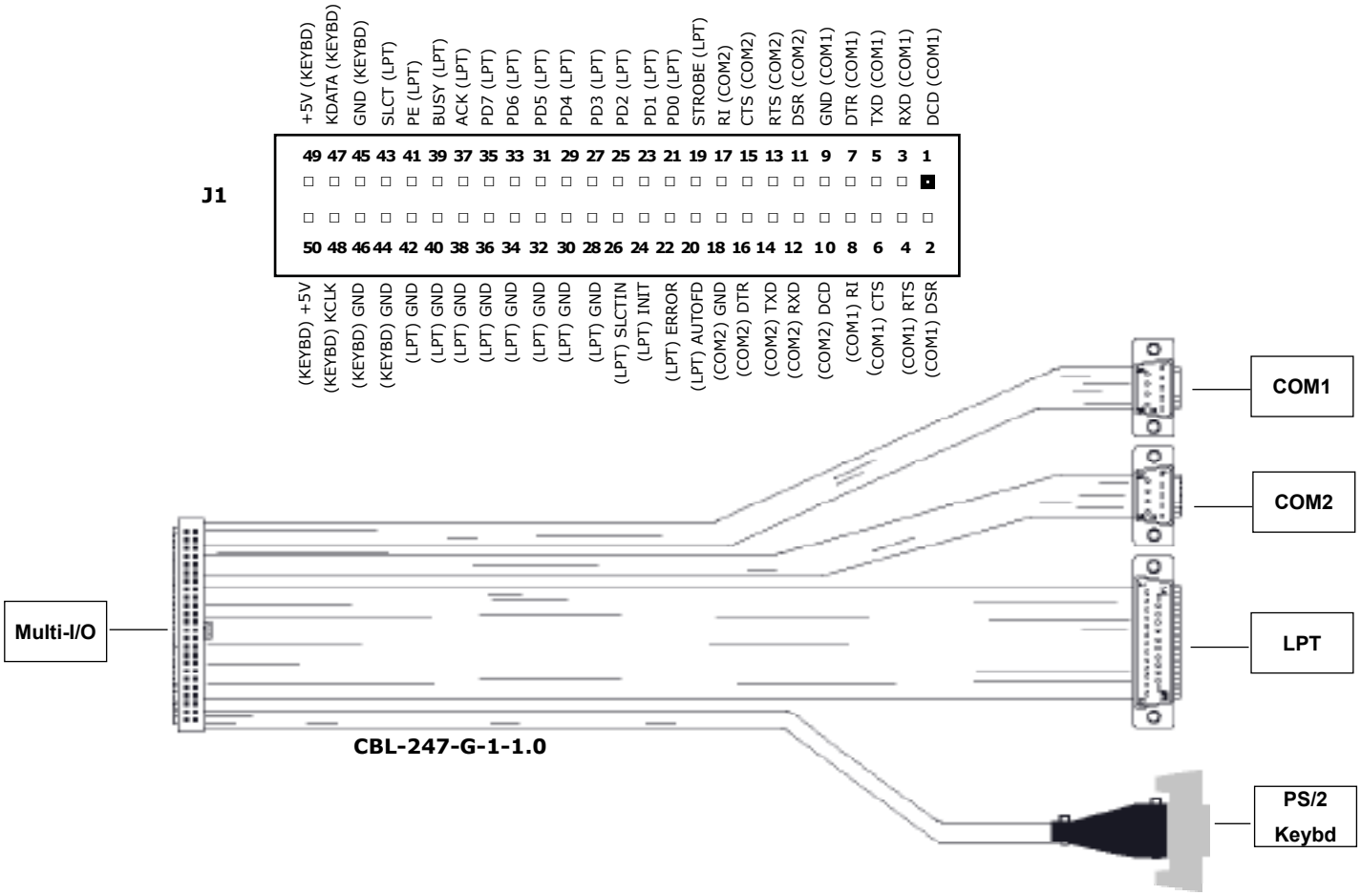
A PS/2 mouse port provides connection for a compatible mouse and is terminated at **J11**. An adapter cable, CBL-343-G-1-1.375, is available from WinSystems to simplify the connection. Optionally, a USB mouse can be connected in addition to, or instead of the standard PS/2 mouse. The pinout for the cable is listed above.

J1 - Multi-I/O (COM1, COM2, Keyboard, LPT)

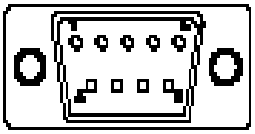
Visual Index

PCB Connector: **TEKA SRC225C425M126-0 (J1)**
Mating Connector: **ITW-PANCON 050-050-455A (Housing)**

The interface to two of the serial ports (COM1/COM2), the printer port and keyboard are all terminated via the connector at **J1**. A cable, part number CBL-247-G-1-1.0, is available from WinSystems to adapt to the conventional I/O connectors. The pinout definition for **J1** is listed below.



COM1, COM2 [DB9 Male]



Pin	RS-232	RS-422	RS-485
1	DCD	N/A	N/A
2	RX	TX+	TX/RX+
3	TX	TX-	TX/RX-
4	DTR	N/A	N/A
5	GND	GND	GND
6	DSR	RX+	N/A
7	RTS	RX-	N/A
8	CTR	N/A	N/A
9	RI	N/A	N/A

All serial ports are configured as Data Terminal Equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO. All serial ports have 16C550-compatible UARTs. The RS-232 transceivers have charge pumps to generate the plus and minus voltages so the PCM-VDX-2-512 only requires +5V to operate.

Each port is setup to provide internal diagnostics such as loopback and echo mode on the data stream. An independent, software programmable baud rate generator is selectable from 50 through 115.2 kbps. Individual modem handshake control signals are supported for all ports.

COM1 and COM2 Configuration Options in BIOS

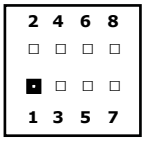
1. RS-232 Mode
2. RS-422 Mode with RTS transmitter enable
3. RS-422 Mode with auto transmitter enable
4. RS-485 Mode with RTS transmitter enable
5. RS-485 Mode with RTS transmitter enable and echo back
6. RS-485 Mode with auto transmitter enable
7. RS-485 Mode with auto transmitter enable and echo back

Mode(s)	Configuration Note
2, 4, 5	Require the RTS bit (MCR Bit 1) to be set in order to transmit.
3, 6, 7	Require TX/RX(300) termination on one node.
4	Requires the RTS (MCR Bit 1) be de-asserted in order to receive.
* Each of the RS-422/RS-485 modes allow for jumper selection of transmit and/or receive termination and biasing resistor(s). An 8-pin configuration jumper is provided for each port.	

Termination Resistors

COM1 = **JP4**

COM2 = **JP2**



RS-422 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX± pair		7-8
RX (100): Places a 100Ω Resistor across the RX± pair		1-2
TX/RX(300):	Places a 100Ω Resistor from +5V to TX+	5-6
	Places a 100Ω Resistor between TX±	7-8
	Places a 100Ω Resistor from Ground to TX-	3-4

RS-485 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX/RX± pair		7-8
TX/RX(300):	Places a 100Ω Resistor from +5V to TX/RX+	5-6
	Places a 100Ω Resistor between TX/RX±	7-8
	Places a 100Ω Resistor from Ground to TX/RX-	3-4

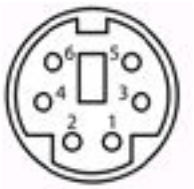
LPT [DB25 Female]

Pin	SPP Signal
1	STROBE
2-9	PD0-PD7
10	ACK
11	BUSY
12	PE
13	SLCT
14	AUTOFD
15	ERROR
16	INIT
17	SLCTIN
18-25	GND

The LPT port is a multimode parallel printer port that supports the PS/2 Standard Bidirectional Parallel Port (SPP), Enhanced Parallel Port (EPP), and Extended Capabilities (ECP) functionality. The output drivers support 8 mA per line.

The printer port can also be used as two additional general-purpose I/O ports if a printer is not required. The first port is configured as eight input or output only lines. The other port is configured as five input and three output lines.

PS/2 Keyboard [6-Position]



Pin	Description
1	KDATA
2	NC
3	GND
4	+5V
5	KCLK
6	NC

This connector supports a PS/2 keyboard interface. The pinout for the cable is listed above.

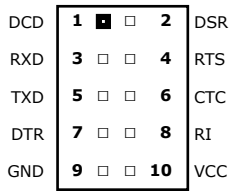
J5 (COM3), J6 (COM4)

Visual Index

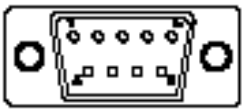
PCB Connector: **MOLEX 87832-1006 (J5, J6)**
Mating Connector: **MOLEX 051110-1060 (Housing)**
MOLEX 50394-8100 (Crimp)

The connectors for COM3 (**J5**) and COM4 (**J6**) are listed below.

RS-232

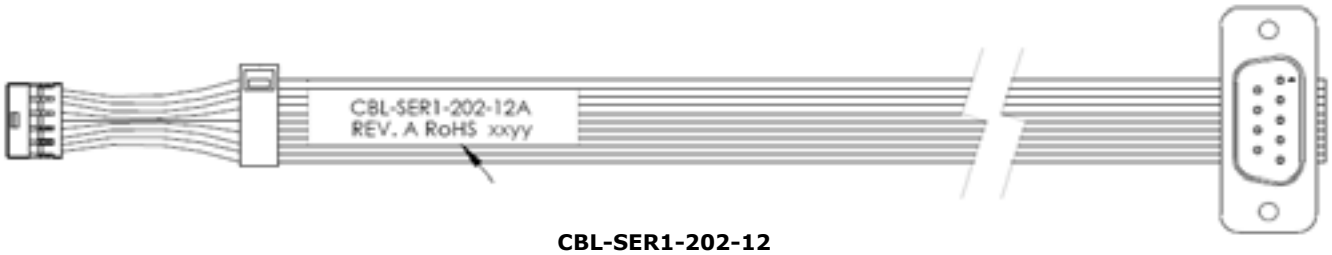


COM3, COM4 [DB9 Male]



Pin	RS-232	RS-422	RS-485
1	DCD	N/A	N/A
2	RX	TX+	TX/RX+
3	TX	TX-	TX/RX-
4	DTR	N/A	N/A
5	GND	GND	GND
6	DSR	RX+	N/A
7	RTS	RX-	N/A
8	CTR	N/A	N/A
9	RI	N/A	N/A

Both ports are configured as Data Terminal Equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO. All serial ports have 16C550-compatible UARTs. The RS-232 has a charge pump to generate the plus and minus voltages so the PCM-VDX-2-512 only requires +5V to operate. An independent, software programmable baud rate generator is selectable from 50 through 115.2 kbps. Individual modem handshake control signals are supported for all ports.



CBL-SER1-202-12

COM3 and COM4 Configuration Options in BIOS

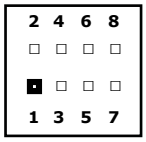
1. RS-232 Mode
2. RS-422 Mode with RTS transmitter enable
3. RS-422 Mode with auto transmitter enable
4. RS-485 Mode with RTS transmitter enable
5. RS-485 Mode with RTS transmitter enable and echo back
6. RS-485 Mode with auto transmitter enable
7. RS-485 Mode with auto transmitter enable and echo back

Mode(s)	Configuration Note
2, 4, 5	Require the RTS bit (MCR Bit 1) to be set in order to transmit.
3, 6, 7	Require TX/RX(300) termination on one node.
4	Requires the RTS (MCR Bit 1) be de-asserted in order to receive.
* Each of the RS-422/RS-485 modes allow for jumper selection of transmit and/or receive termination and biasing resistor(s). An 8-pin configuration jumper is provided for each port.	

Termination Resistors

COM3 = **JP1**

COM4 = **JP3**



RS-422 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX± pair		7-8
RX (100): Places a 100Ω Resistor across the RX± pair		1-2
TX/RX(300):	Places a 100Ω Resistor from +5V to TX+	5-6
	Places a 100Ω Resistor between TX±	7-8
	Places a 100Ω Resistor from Ground to TX-	3-4

Revision prior to E PCB products require a wire-wrap jumper from 2-3.

Revision prior to E PCB products require a wire-wrap jumper from 1-4.

RS-485 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX/RX± pair		7-8
TX/RX(300):	Places a 100Ω Resistor from +5V to TX/RX+	5-6
	Places a 100Ω Resistor between TX/RX±	7-8
	Places a 100Ω Resistor from Ground to TX/RX-	3-4

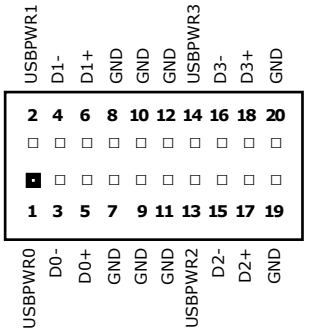
Revision prior to E products require a wire-wrap jumper from 1-4.

J15 - USB

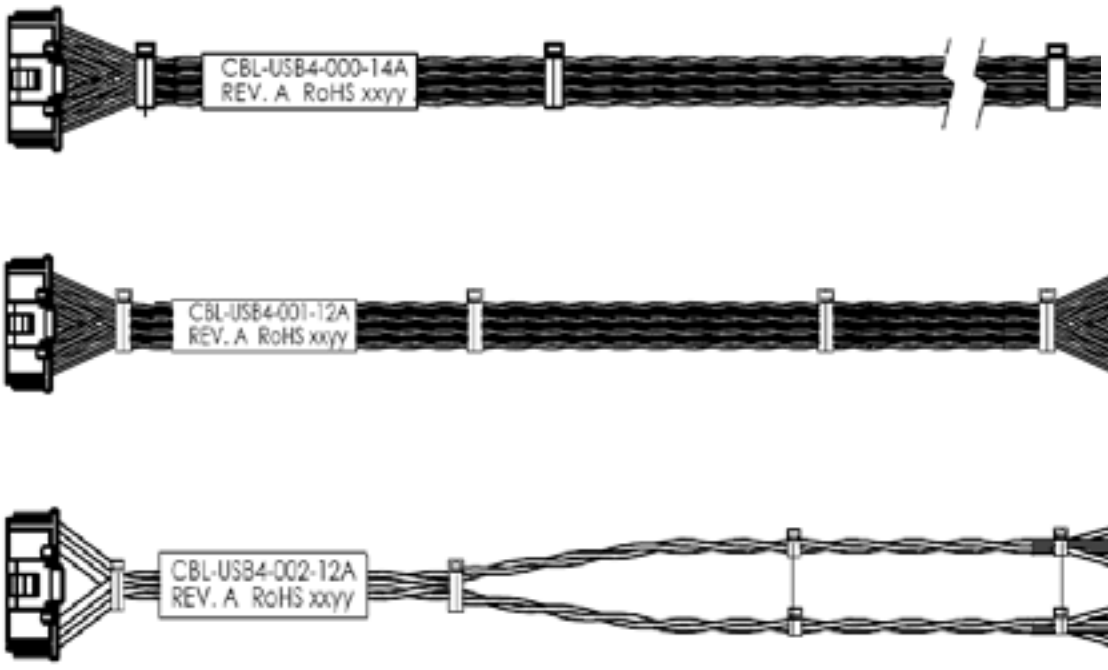
Visual Index

PCB Connector: **MOLEX 501571-2007 (J15)**
Mating Connector: **MOLEX 501189-2010 (Housing)**
MOLEX 501193-2000 (Crimp)

J15
(USB 0/1/2/3)



CBL-USB4-000-14, CBL-USB4-001-12, CBL-USB4-002-12



A USB cable may be attached to the PCM-VDX-2-512 via the connector for a total of four USB 2.0 ports. Adapter cables CBL-USB4-000-14, CBL-USB4-001-12, and CBL-USB4-002-12 are available from WinSystems for connection.

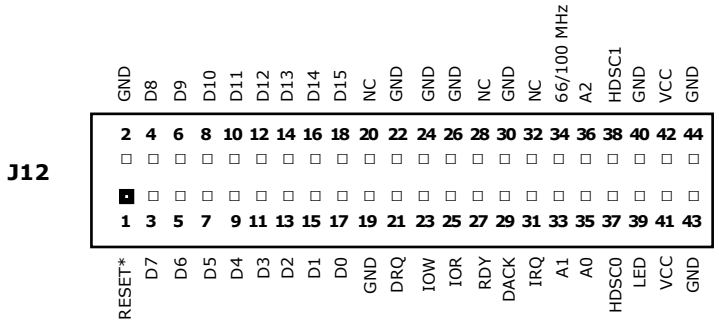
PARALLEL ATA

J12 - PATA

Visual Index

PCB Connector: **SAMTEC STMM-122-02-G-D-SM-P-TR (J12)**

Mating Connector: **SAMTEC ASP-129789-01**



The PCM-VDX-2-512 supports the PATA interface at **J12** (44-pin primary). WinSystems offers cable CBL-266-G-2-0.75 to simplify this connection.

COMPACTFLASH

J101 - COMPACTFLASH

Visual Index

When using a CompactFlash device, Master/Slave selection is made using jumper field **JP5**. The PCM-VDX-2-512 supports solid state CompactFlash storage devices for applications where the environment is too harsh for mechanical hard disks.

The CompactFlash socket at **J101** supports modules with TrueIDE support. WinSystems offers industrial grade CompactFlash modules that provide high performance and extended temperature operation (-40ºC to +85ºC). A PATA activity LED is present at **D9**.

The CompactFlash is a PATA device. Use of a CompactFlash device therefore reduces the number of available PATA devices to one.

MICRO SD

J10 - MicroSD (Minimum Order Quantity Required)

Visual Index

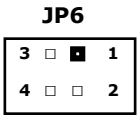
JP5 - SSD Options

The PCM-VDX-2-512 can be populated with an optional MicroSD socket at **J10**. The bootable MicroSD socket shares some signals with the PATA controller and cannot be used in conjunction with other PATA devices. The PATA interface, CompactFlash and on-board Silicon-Disk cannot be used at the same time as the MicroSD card.

A jumper at **JP5** 9-10 allows read/write access to the MicroSD card. When **JP5** pins 9 and 10 are open, the MicroSD is write protected and operating in read-only mode.

JP6 - SSD Enable/Disabled

Visual Index



SSD Enabled	1-2, 3-4
SSD Disabled	1 2 , 3 4

Optional On-board Flash Disk

The PCM-VDX-2-512M can be populated with an optional on-board Flash disk for rugged OEM applications where a removal device is not desirable. The Flash disk is connected to the PATA controller but must be enabled by installing jumpers at **JP6** 1-2, 3-4. Removing the jumpers at **JP6** 1 2, and 3 4, effectively removes the device from the PATA bus, giving the user the ability to connect two additional devices to the PATA controller. Since the on-board Flash disk may co-exist with another PATA device, it can be set as Master by installing a jumper at **JP5** pins 3-4 or Slave when the **JP5** pins 3 and 4 are open.

A jumper at **JP5** 5-6 write protects the on-board Flash disk. When **JP5** pins 5 and 6 are open, read/write access is available to the on-board Flash disk.

Please contact an Applications Engineer if you are interested in this optional feature.

NOTE: SRAM is not applicable for model PCM-VDX-1-256.

The PCM-VDX-2-512 board provides 1 MB of battery-backed user SRAM. The 1 MB SRAM is normally used as a solid state disk device by using the appropriate driver for your operating systems.

For example, the DOS driver **USSD.SYS** can be used to make the SRAM appear as a drive in the system by adding the following to **config.sys**.

Device = c:\ussd.sys /mod:u /pad:220 /dsz:1024

The base address for the SRAM is located at 0220h.

There are four I/O registers used for accessing the memory array. The register definition and usage is defined below.

OFFSET 0 - MSB Address Register
D7 - A23 of access address
D6 - A22 of access address
D5 - A21 of access address
D4 - A20 of access address
D3 - A19 of access address
D2 - A18 of access address
D1 - A17 of access address
D0 - A16 of access address

This register is write-only and holds the upper 8 bits of the 24-bit address used to access the 1 MB SRAM.

OFFSET 1 - NSB Address Register
D7 - A15 of access address
D6 - A14 of access address
D5 - A13 of access address
D4 - A12 of access address
D3 - A11 of access address
D2 - A10 of access address
D1 - A9 of access address
D0 - A8 of access address

This register is write-only and holds the middle 8 bits of address used to access the 1 MB memory array. Writing this register also clears the LSB address counter to 0.

OFFSET 2 - Data Access Register A
D7 - D7 of memory data
D6 - D6 of memory data
D5 - D5 of memory data
D4 - D4 of memory data
D3 - D3 of memory data
D2 - D2 of memory data
D1 - D1 of memory data
D0 - D0 of memory data

This read/write register is the primary window to the memory array. A value written to this port will be written to the address in the memory array specified by the MSB register, the NSB register, and the current LSB counter address. In like fashion, a read from this I/O address will result in the current memory array data at the address specified by the MSB register, the NSB register, and the LSB address counter. In either case, read or write, an access to this register results in the LSB address counter being incremented immediately following the access so that the next access will be at the next sequential address in the array. This incrementing process does **not** carry into the NSB or MSB register which must be rewritten every 256 bytes.

OFFSET 3 - Data Access Register B
D7 - D7 of memory data
D6 - D6 of memory data
D5 - D5 of memory data
D4 - D4 of memory data
D3 - D3 of memory data
D2 - D2 of memory data
D1 - D1 of memory data
D0 - D0 of memory data

This read/write register is used to access the memory array when post incrementing of the LSB counter is not desired. The byte written or read will still be specified by the 24-bit combination of the MSB register, the NSB register, and the LSB counter. However, the LSB counter will **not** be altered following the access. It will then be necessary to do one more read from Data Access Register A in order to bump the address to the next byte.

OFFSET 4 - Write Protect Register
D7 - D6 - Reserved
D0 - Write Protect Bit, 0 = Protected, 1 = Writeable

This write-only register controls the write protect function of the 1 MB SRAM board. On power up, the write protect bit is cleared (disabling writes) and must be explicitly enabled by writing a **1** to the I/O port at the BASE address +4. To re-enable the write protection, write a **0** at this register. The **USSD.SYS** device will enable writing only during that time when a sector is being transferred, which contributes greatly to data safety and integrity.

J2, J13 - 10/100 Mbps Ethernet

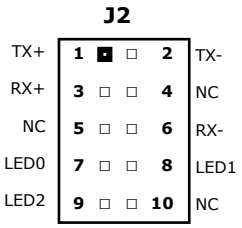
Visual Index

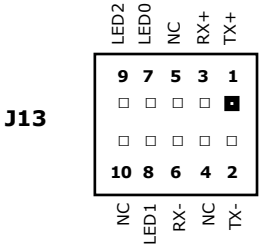
PCB Connector: **MOLEX 87832-1006 (J2, J13)**
MOLEX 51110-1051 (Housing)
MOLEX 50394-8100 (Crimp)

10/100 Mbps Ethernet Controllers

The PCM-VDX-2-512 is equipped with a Realtek 8100C Ethernet controller **(J13)** and a Vortex86DX LAN controller **(J2)**. Each provides a standard IEEE 802.3 Ethernet interface for 100/10BASE-T networks.

On-board Ethernet activity LEDs **D1 and D2** are provided. See tables below for signal and pin definitions.





J2 (Ethernet Port 1) Indicators

LED	Color	Signal	Off-board
D2	YELLOW	LINK/ACTIVITY	LED0, LED1
D1	RED	SPEED	LED2

J13 (Ethernet Port 2) Indicators

LED	Color	Signal	Off-board
D14	GREEN	LINK	LED0
D18	RED	SPEED100	LED2
D15	YELLOW	ACTIVITY	LED1

CBL-ENET1-202-12

CBL-ENET1-203-12

D21 - Status LED

Visual Index

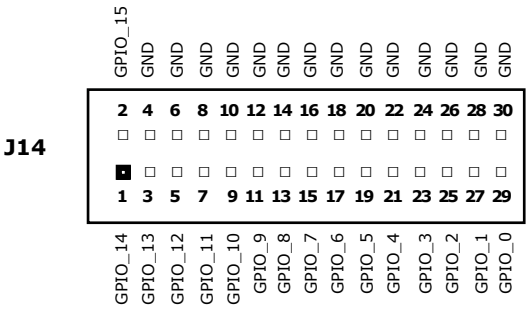
A status LED is populated on the board at **D21** which can be used for any application specific purpose. The LED can be turned on in software applications by writing a **1** to I/O port 1EDH. The LED can be turned off by writing a **0** to 1EDH. The Activity LED will turn on and off as packets are received and transmitted.

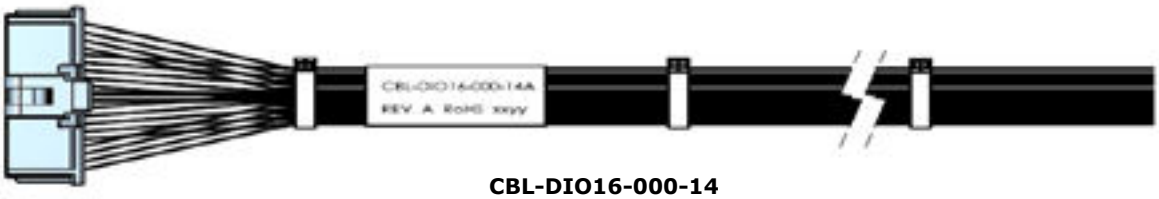
D21	--	GREEN	STATUS

J14 - GPIO

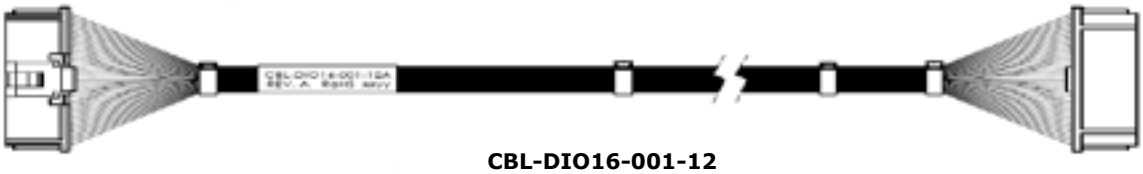
Visual Index

PCB Connector: MOLEX 501571-3007 (J14)
Mating Connector: MOLEX 501189-3010 (Housing)
MOLEX 501193-2000 (Crimp)

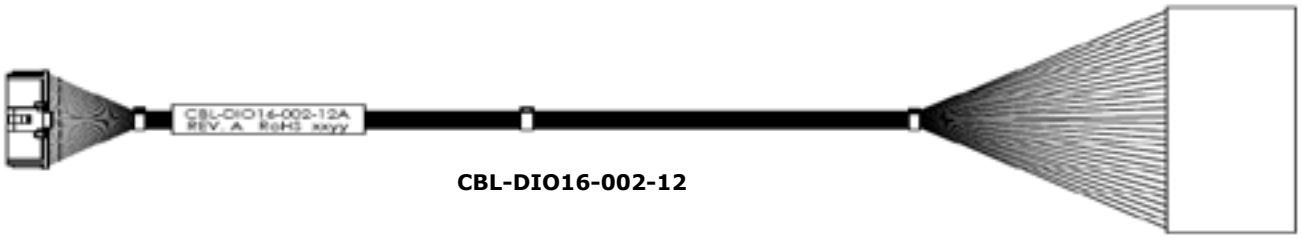




CBL-DIO16-000-14



CBL-DIO16-001-12



CBL-DIO16-002-12

The PCM-VDX-2-512 Digital I/O consists of sixteen dedicated programmable I/O pins consisting of two individual 8-bit ports. Each port can be confugred as GPIO or Pulse Width Modulation (PWM) outputs.

All GPIO pins are independent and can be configured as inputs or outputs. When configured as outputs, pins have 8 mA drive capability and are unterminated. When configured as inputs, pins are pulled-high with a 75k Ω resistance. Each input pin also supports interrupt triggers.

All PWM pins are independent and can be configured to output a continuous frequency or a fixed number of pulses. The frequency is selected by programming high and low pulse count values. An interrupt can be used to indicate when a pulse count has completed.

The features are configured and controlled utilizing PCI configuration and I/O access instructions.

Setup GPIO Registers

	Port 0	Port 1	Description
Data Register	78H	79H	
Direction Register	98H	99H	0: GPIO pin is input mode 1: GPIO pin is output mode

If send value 0FH to port 98H, it means that GPIO port 0 [7-4] are input mode and port[3-0] are output mode.

If send value 00H to port 98H, it means that GPIO port 0 [7-0] are input mode.

If send value FFH to port 98H, it means that GPIO port 0 [7-0] are output mode.

If send value 03H to port 98H, it means that GPIO port 0 [7-2] are input mode and port[1-0] are output mode.

GPIO with Interrupt

The Vortex86DX GPIO ports 0 and 1 support interrupt trigger. To save CPU performance, interrupt can be used instead of polling GPIO. GPIO port 0 interrupt registers are at offset DCh~DFh south bridge and GPIO1 registers are at offset E0h~E3h.

Steps to setup GPIO to trigger interrupt:

1. Configure interrupt mask register to determine which GPI can trigger interrupt individually.
2. Set trigger level (high or low) for each GPI.
3. Set period time that interrupt will be generated while the event loading time of any one of GPI[7-0] is longer than the time parameters.
4. Select IRQ.
5. Set interrupt trigger once or continuously.

For more information on programming GPIO, see **Software Drivers & Examples** section on our website.

J3, J7 - PC/104

Visual Index

PCB Connector: **TEKA SBL PC232-A-1A7-M (J3)**
TEKA SBL PC220-A-1A7-M (J7)

The PC/104 bus is electrically equivalent to the 16-bit ISA bus. Standard PC/104 I/O cards can be populated on PCM-VDX-2-512's connectors, located at **J3** and **J7**. The interface does not support hot swap capability. The PC/104 bus connector pin definitions are provided below for reference. Refer to the PC/104 Bus Specification for specific signal and mechanical specifications.

J7 (C/D)

GND	**D0**	**C0**	GND
MEMCS16#	**D1**	**C1**	SBHE#
IOCS16#	**D2**	**C2**	LA23
IRQ10	**D3**	**C3**	LA22
IRQ11	**D4**	**C4**	LA21
IRQ12	**D5**	**C5**	LA20
IRQ15	**D6**	**C6**	LA19
IRQ14	**D7**	**C7**	LA18
DACK0#	**D8**	**C8**	LA17
DRQ0	**D9**	**C9**	MEMR#
DACK5#	**D10**	**C10**	MEMW#
DRQ5	**D11**	**C11**	SD8
DACK6#	**D12**	**C12**	SB9
DRQ6	**D13**	**C13**	SD10
DACK7#	**D14**	**C14**	SD11
DRQ7	**D15**	**C15**	SD12
+5V	**D16**	**C16**	SD13
MASTER#	**D17**	**C17**	SD14
GND	**D18**	**C18**	SD15
GND	**D19**	**C19**	KEY

J3 (A/B)

IOCHK#	**A1**	**B1**	GND
SD7	**A2**	**B2**	RESET
SD6	**A3**	**B3**	+5V
SD5	**A4**	**B4**	IRQ
SD4	**A5**	**B5**	-5V
SD3	**A6**	**B6**	DRQ2
SD2	**A7**	**B7**	-12V
SD1	**A8**	**B8**	SRDY#
SD0	**A9**	**B9**	+12V
IOCHRDY	**A10**	**B10**	KEY
AEN	**A11**	**B11**	SMEMW#
SA19	**A12**	**B12**	SMEMR#
SA18	**A13**	**B13**	IOW#
SA17	**A14**	**B14**	IOR#
SA16	**A15**	**B15**	DACK3#
SA15	**A16**	**B16**	DRQ3
SA14	**A17**	**B17**	DACK1#
SA13	**A18**	**B18**	DRQ1
SA12	**A19**	**B19**	REFRESH#
SA11	**A20**	**B20**	BCLK
SA10	**A21**	**B21**	IRQ7
SA9	**A22**	**B22**	IRQ6
SA8	**A23**	**B23**	IRQ5
SA7	**A24**	**B24**	IRQ4
SA6	**A25**	**B25**	IRQ3
SA5	**A26**	**B26**	DACK2#
SA4	**A27**	**B27**	TC
SA3	**A28**	**B28**	BALE
SA2	**A29**	**B29**	+5V
SA1	**A30**	**B30**	OSC
SA0	**A31**	**B31**	GND
GND	**A32**	**B32**	GND

= Active Low Signal

NOTES:

1. Rows C and D are not required on 8-bit modules.
2. B10 and C19 are key locations. WinSystems uses key pins as connections to GND.
3. Signal timing and function are as specified in ISA specification.
4. Signal source/sink current differ from ISA values.

J102 - MiniPCI Socket

Visual Index

The PCM-VDX-2-512 includes a MiniPCI socket at **J102**. Though the socket can support other devices, it is primarily intended for adding a video module. WinSystems offers MPCI-VGA-Z9S to simplify the connection. Additionally, wireless activity is optional via MiniPCI.

MiniPCI Device Interface (CN1)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	N/C	2	N/C	63	3.3V	64	FRAME#
	KEY		KEY	65	CLKRUN#	66	TRDY#
3	N/C	4	N/C	67	SERR#	68	STOP#
5	N/C	6	N/C	69	GROUND	70	3.3V
7	N/C	8	N/C	71	PERR#	72	DEVSEL#
9	N/C	10	N/C	73	C/BE(1)#	74	GROUND
11	N/C	12	N/C	75	AD(14)	76	AD(15)
13	N/C	14	N/C	77	GROUND	78	AD(13)
15	N/C	16	RESERVED	79	AD(12)	80	AD(11)
17	INTB#	18	5V	81	AD(10)	82	GROUND
19	3.3V	20	INTA#	83	GROUND	84	AD(09)
21	RESERVED	22	RESERVED	85	AD(08)	86	C/BE(0)#
23	GROUND	24	3.3V AUX	87	AD(07)	88	3.3V
25	CLK	26	RST#	89	3.3V	90	AD(06)
27	GROUND	28	3.3V	91	AD(05)	92	AD(04)
29	REQ#	30	GNT#	93	RESERVED	94	AD(02)
31	3.3V	32	GROUND	95	AD(03)	96	AD(00)
33	AD(31)	34	PME#	97	5V	98	RESERVED_WIP[5]
35	AD(29)	36	RESERVED	99	AD(01)	100	RESERVED_WIP[5]
37	GROUND	38	AD(30)	101	GROUND	102	GROUND
39	AD(27)	40	3.3V	103	N/C	104	M66EN
41	AD(25)	42	AD(28)	105	N/C	106	N/C
43	RESERVED	44	AD(26)	107	N/C	108	N/C
45	C/BE(3)#	46	AD(24)	109	N/C	110	N/C
47	AD(23)	48	IDSEL	111	N/C	112	RESERVED_WIP5
49	GROUND	50	GROUND	113	N/C	114	GROUND
51	AD(21)	52	AD(22)	115	N/C	116	N/C
53	AD(19)	54	AD(20)	117	N/C	118	N/C
55	GROUND	56	PAR	119	N/C	120	N/C
57	AD(17)	58	AD(18)	121	RESERVED	122	N/C
59	C/BE(2)#	60	AD(16)	123	N/C	124	3.3V AUX
61	IRDY#	62	GROUND				

General Information

The PCM-VDX-2-512 includes an AMI BIOS to assure full compatibility with PC operating systems and software. The basic system configuration is stored in battery backed CMOS RAM within the clock/calendar. As an alternative, the BIOS configuration may be stored in internal Flash for operation without a battery. For more information on CMOS configuration, see the BIOS Settings Storage Options section of this manual.

Entering Setup

To enter setup, power up the computer and press **Delete** to enter the setup menu. It may take a few seconds before the main setup menu screen is displayed.

Navigation of the Menus

Use the **Up** and **Down** arrow keys to move among the selections and press **Enter** when a selection is highlighted to enter a sub-menu or to see a list of choices. Following are images of each menu screen in the default configuration along with a brief description of each option where applicable. Available options are listed in reference tables. Menu values shown in **bold** typeface are factory defaults.

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Main Menu	
System Overview	
Processor	
Vortex86DX A9121	
Speed:	1000 MHz
System Memory	
Size:	512MB
Speed:	333MHz
System Time	**[05:09:58]**
System Date:	**[Tue 08/12/2010]**

Each available option is listed in detail in the following sections.

Navigation to the screens is located at the top of each screen's layout.

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Advanced	
Advanced Settings	
WARNING: Setting wrong values in below sections may cause system to malfunction.	
> CPU Configuration	
> IDE Configuration	
> Remote Access Configuration	
> USB Configuration	
SB LAN	**Enabled**
Options: Enabled Disabled	
MAC Address	**[xx xx xx xx xx xx]**

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Advanced > CPU Configuration	
Module Version - 00.01	
Manufacturer:	DMP
Brand String:	Vortex86DX A9121
Frequency:	1.00 GHz
L1 Cache	**Enabled**
Options: Disabled Enabled	
Cache L1:	16 KB
L2 Cache	**Write-Thru**
Options: Disabled Write-Thru Write-Back	
Fetch Line Size	**4 DWORD**
Options: 4 DWORD 8 DWORD	
Cache L2:	256 KB
CPU Speed Setting By	**Divide By 1**
Options: Divide By 1 Divide By 2 Divide By 3 Divide By 4 Divide By 5 Divide By 8 Divide By 16 Divide By 32	
CPU Fast Decode Onboard Cycle	**Normal**
Options: Normal Fast	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Advanced > **IDE Configuration**	
Onboard PCI IDE Controller	**Primary**
Options: Disabled Primary	
> Primary IDE Master	**Auto***
> Primary IDE Slave	**Auto***
*Standard devices are automatically detected.	
Hard Disk Write Protect	**Disabled**
Options: Disabled Enabled	
IDE Detect Time Out (Sec)	**35**
Options: 0 5 10 15 20 25 30 35	
ATA(PI) 80Pin Cable Detection	**Host & Device**
Options: Host & Device Host Device	
Hard Disk Delay	**2 Second**
Options: Disabled 1 Second 2 Second 4 Second 8 Second	
OnBoard IDE Operate Mode	**Legacy Mode**
Options: Legacy Mode Native Mode	
Standard IDE Compatible	**Disabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Advanced > IDE Configuration > **Primary IDE Master**	
Device:	Auto-Detected
Type	**Auto**
Options: Not Installed Auto CD/DVD ARMD	
LBA/Large Mode	**Auto**
Options: Disabled Auto	
Block (Multi-Sector Transfer)	**Auto**
Options: Disabled Auto	
PIO Mode	**Auto**
Options: Auto 0 1 2 3 4	
DMA Mode	**Auto**
Options: Auto SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2	
S.M.A.R.T.	**Auto**
Options: Auto Disabled Enabled	
32Bit Data Transfer	**Enabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Advanced > IDE Configuration > **Primary IDE Slave**	
Device:	Auto-Detected
Type	**Auto**
Options: Not Installed Auto CD/DVD ARMD	
LBA/Large Mode	**Auto**
Options: Disabled Auto	
Block (Multi-Sector Transfer)	**Auto**
Options: Disabled Auto	
PIO Mode	**Auto**
Options: Auto 0 1 2 3 4	
DMA Mode	**Auto**
Options: Auto SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2	
S.M.A.R.T.	**Auto**
Options: Auto Disabled Enabled	
32Bit Data Transfer	**Enabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Advanced > Remote Access Configuration	
Configure Remote Access type and parameters	
Remote Access	**Disabled**
Options: Disabled Enabled	
The following selections are available only with Remote Access enabled.	
Serial Port number	**COM1**
Options: COM1 COM2 COM3 COM4	
Base Address, IRQ	**3F8h, 4**
Serial Port Mode	**115200 8,n,1**
Options: 115200 8,n,1 57600 8,n,1 38400 8,n,1 19200 8,n,1 09600 8,n,1	
Flow Control	**None**
Options: None Hardware Software	
Redirection After BIOS POST	**Always**
Options: Disabled Boot Loader Always	
Terminal Type	**ANSI**
Options: ANSI VT100 VT-UTF8	
VT-UTF8 Combo Key Support	**Enabled**
Options: Disabled Enabled	
Sredir Memory Display Delay	**No Delay**
Options: No Delay Delay 1 Sec Delay 2 Sec Delay 4 Sec	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Advanced > **USB Configuration**	
Module Version - 2.24.2-13.4	
USB Devices Enabled	**Auto-Detected**
USB Port 0,1	**Enabled**
Options: Enabled Disabled	
USB Port 2,3	**Enabled**
Options: Enabled Disabled	
USB 2.0 Controller Mode	**HiSpeed**
Options: FullSpeed HiSpeed	
BIOS EHCI Hand-Off	**Enabled**
Options: Disabled Enabled	
USB Beep Message	**Enabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

PCIPnP	
Advanced PCI/PnP Settings	
Warning: Setting wrong values in below sections may cause system to malfunction.	
Plug & Play O/S	**No**
Options: No Yes	
PCI Latency Timer	**128**
Options: 32 64 96 128 160 192 224 248	
Allocate IRQ to PCI VGA	**No**
Options: Yes No	
Palette Snooping	**Disabled**
Options: Disabled Enabled	
PCI IDE BusMaster	**Enabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

PCIPnP (cont'd)	
IRQ3	**Reserved**
Options: Available Reserved	
IRQ4	**Reserved**
Options: Available Reserved	
IRQ5	**Available**
Options: Available Reserved	
IRQ6	**Available**
Options: Available Reserved	
IRQ7	**Available**
Options: Available Reserved	
IRQ9	**Available**
Options: Available Reserved	
IRQ10	**Available**
Options: Available Reserved	
IRQ11	**Available**
Options: Available Reserved	
IRQ12	**Available**
Options: Available Reserved	
IRQ15	**Available**
Options: Available Reserved	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

PCIPnP (cont'd)	
DMA Channel 0	**Available**
Options: Available Reserved	
DMA Channel 1	**Available**
Options: Available Reserved	
DMA Channel 3	**Available**
Options: Available Reserved	
DMA Channel 5	**Available**
Options: Available Reserved	
DMA Channel 6	**Available**
Options: Available Reserved	
DMA Channel 7	**Available**
Options: Available Reserved	
Reserved Memory Size	**Disabled**
Options: Disabled 16k 32k 64k	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Boot	
Boot Settings	
> Boot Settings Configuration	
1st Boot Device	**Disabled**

The PCM-VDX-2-512 BIOS will not display devices which are not connected, regardless of their location in the boot order. The boot order can be adjusted by connecting ALL the desired media devices, setting the boot order and then selecting **Save Custom Defaults**.

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Boot > Boot Settings Configuration

Boot Settings Configuration	
Quick Boot	**Enabled**
Options: Disabled Enabled	
Quiet Boot	**Disabled**
Options: Disabled Enabled	
Bootup Num-Lock	**On**
Options: Off On	
PS/2 Mouse Support	**Auto**
Options: Disabled Enabled Auto	
Interrupt 19 Capture	**Enabled**
Options: Disabled Enabled	
Boot From LAN	**Disabled**
Options: Disabled Used INT 18h Used INT 19h PnP/BEV(BBS) RPL	
Beep Function	**Disabled**
Options: Enabled Disabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Security	
Supervisor Password Is:	**Not Installed**
User Password Is:	**Not Installed**
Change Supervisor Password	
Change User Password	
Boot Sector Virus Protection	**Disabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Chipset
Advanced Chipset Settings
Warning: Setting wrong values in below sections may cause system to malfunction.
> NorthBridge Configuration
> SouthBridge Configuration

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Chipset > **NorthBridge Chipset Configuration**	
DRAM Timing Setting By	**BIOS**
Options: Manual BIOS	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Chipset > **SouthBridge Chipset Configuration**	
P.O.S.T. Forward To	**Disabled**
Options: Disabled COM1	
> ISA Configuration	
> Serial/Parallel Port Configuration	
> WatchDog Configuration	
> Multi-Function Port Configuration	
> Redundancy Control Configuration	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Chipset > SouthBridge Chipset Configuration > **ISA Configuration**	
ISA Clock	**8.3MHz**
Options: 8.3MHz 16.6MHz	
ISA 16bits I/O wait-state	**1 clock**
Options: 1 clock 2 clock 3 clock 4 clock 5 clock 6 clock 7 clock 8 clock	
ISA 8bits I/O wait-state	**4 clock**
Options: 1 clock 2 clock 3 clock 4 clock 5 clock 6 clock 7 clock 8 clock	
ISA 16bits Memory wait-state	**1 clock**
Options: 0 clock 1 clock 2 clock 3 clock 4 clock 5 clock 6 clock 7 clock	
ISA 8bits Memory wait-state	**4 clock**
Options: 1 clock 2 clock 3 clock 4 clock 5 clock 6 clock 7 clock 8 clock	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Chipset > SouthBridge Chipset Configuration > **Serial/Parallel Port Configuration**

SB Serial Port 1	**3F8**
Options: Disabled 3F8 2F8 3E8 2E8	
Serial Port IRQ 1	**IRQ 4**
Options: IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ9 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15	
Serial Port Baud Rate	**115200 BPS**
Options: 2400 BPS 4800 BPS 9600 BPS 19200 BPS 38400 BPS 57600 BPS 115200 BPS	
SB Serial Port 2	**2F8**
Options: Disabled 3F8 2F8 3E8 2E8	
Serial Port IRQ 2	**IRQ3**
Options: IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ9 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15	
Serial Port Baud Rate	**115200 BPS**
Options: 2400 BPS 4800 BPS 9600 BPS 19200 BPS 38400 BPS 57600 BPS 115200 BPS	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Chipset > SouthBridge Chipset Configuration >
Serial/Parallel Port Configuration (cont'd)

SB Serial Port 3	**3E8**
Options: Disabled 3E8 2E8 3A8 2A8	
Serial Port IRQ 3	**IRQ 9**
Options: IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ9 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15	
Serial Port Baud Rate	**115200 BPS**
Options: 2400 BPS 4800 BPS 9600 BPS 19200 BPS 38400 BPS 57600 BPS 115200 BPS	
SB Serial Port 4	**2E8**
Options: Disabled 3E8 2E8 3A8 2A8	
Serial Port IRQ 4	**IRQ11**
Options: IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ9 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15	
Serial Port Baud Rate	**115200 BPS**
Options: 2400 BPS 4800 BPS 9600 BPS 19200 BPS 38400 BPS 57600 BPS 115200 BPS	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Chipset > SouthBridge Chipset Configuration > **Serial/Parallel Port Configuration (cont'd)**	
SB Parallel Port Address	**378**
Options: Disabled 378 278	
Parallel Port Mode	**EPP 1.7 AND SPP**
Options: BPP EPP 1.9 AND SPP ECP ECP AND EPP 1.9 SPP EPP 1.7 AND SPP ECP AND EPP 1.7	
Parallel Port IRQ	**IRQ7**
Options: IRQ5 IRQ7	
SB Serial Port 1 Mode	**RS232**
Options: RS232 RS422 RTS RS422 AUTO RS485 RTS RS485 RTS+ECHO RS485 AUTO RS485 AUTO+ECHO	
SB Serial Port 2 Mode	**RS232**
Options: RS232 RS422 RTS RS422 AUTO RS485 RTS RS485 RTS+ECHO RS485 AUTO RS485 AUTO+ECHO	
SB Serial Port 3 Mode	**RS232**
Options: RS232 RS422 RTS RS422 AUTO RS485 RTS RS485 RTS+ECHO RS485 AUTO RS485 AUTO+ECHO	
SB Serial Port 4 Mode	**RS232**
Options: RS232 RS422 RTS RS422 AUTO RS485 RTS RS485 RTS+ECHO RS485 AUTO RS485 AUTO+ECHO	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Chipset > SouthBridge Chipset Configuration >
WatchDog Configuration

Watchdog Timer	**0**

Options:
0
2 Sec
20 Sec
200 Sec

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Chipset > SouthBridge Chipset Configuration > **Multi-Function Port Configuration**	
Port0 Function	**GPIO**
Options: GPIO 8051 P0 PWM00..PWM07	
Port0 Bit0 Direction	**IN**
Options: IN OUT	
Port0 Bit1 Direction	**IN**
Options: IN OUT	
Port0 Bit2 Direction	**IN**
Options: IN OUT	
Port0 Bit3 Direction	**IN**
Options: IN OUT	
Port0 Bit4 Direction	**IN**
Options: IN OUT	
Port0 Bit5 Direction	**IN**
Options: IN OUT	
Port0 Bit6 Direction	**IN**
Options: IN OUT	
Port0 Bit7 Direction	**IN**
Options: IN OUT	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Chipset > SouthBridge Chipset Configuration > **Multi-Function Port Configuration (cont'd)**	
Port1 Function	**GPIO**
Options: GPIO 8051 P1 PWM08..PWM15	
Port1 Bit0 Direction	**IN**
Options: IN OUT	
Port1 Bit1 Direction	**IN**
Options: IN OUT	
Port1 Bit2 Direction	**IN**
Options: IN OUT	
Port1 Bit3 Direction	**IN**
Options: IN OUT	
Port1 Bit4 Direction	**IN**
Options: IN OUT	
Port1 Bit5 Direction	**IN**
Options: IN OUT	
Port1 Bit6 Direction	**IN**
Options: IN OUT	
Port1 Bit7 Direction	**IN**
Options: IN OUT	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Chipset > SouthBridge Chipset Configuration > **Redundancy Control Configuration**	
Dual Port 4KB SRAM	**Disabled**
Options: Enabled Disabled	
Invalid OPCODE Condition	**Disabled**
Options: Disabled Enabled	
KB/MS System Fail	**Normal**
Options: Normal TRI-State	
GPIO PORT0 System Fail	**Normal**
Options: Normal TRI-State	
GPIO PORT1 System Fail	**Normal**
Options: Normal TRI-State	
LPT PORT System Fail	**Normal**
Options: Normal TRI-State	
UART1 System Fail	**Normal**
Options: Normal TRI-State	
UART2 System Fail	**Normal**
Options: Normal TRI-State	
UART3 System Fail	**Normal**
Options: Normal TRI-State	
UART4 System Fail	**Normal**
Options: Normal TRI-State	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Exit
Save Changes and Exit
Discard Changes and Exit
Discard Changes
Load Factory Defaults
Save Custom Defaults
Load Custom Defaults

BIOS SETTINGS STORAGE OPTIONS

CMOS Storage Locations

The PCM-VDX-2-512's BIOS configuration is stored in three (3) locations:

(1) CMOS RAM (nonvolatile if battery backed)

(2) FLASH PROM (nonvolatile storage for factory defaults)

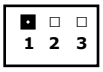
(3) Internal Flash (for custom settings)

Saving the CMOS Configuration

The Real-Time Clock and the CMOS RAM settings can be maintained by an optional battery when the board is powered off. When the external battery is used, simply disconnect the battery from **J8** for 20 seconds. When an optional on-board battery is used, it can be enabled or disabled at **JP7**. A battery is always required to maintain time and date functions when the board is powered off.

Master Battery Enable

JP7



Enables On-board Battery*	1-2
Enables External Battery (default)	1 2
NC	2-3

***Applicable to OEM models only.**

CABLES

Part Number	Description
CBL-SET-373-G-2	Cable set for PCM-VDX-2-512 includes:
CBL-174-G-1-1.5	18-in., 8-wire power cable
CBL-247-G-1-1.0	1-ft., Multi-I/O adapter
CBL-SER1-202-12	Serial I/O Cable (COM3/COM4)
CBL-USB4-002-12	4x USB ports to two, 2-mm 2x4 connectors
CBL-ENET1-204-12	2-mm 2x5 to 2-mm 2x6 connector (2 each)
ADP-IO-G-EBC0364	2 Ethernet, 4 USB
BAT-LTC-E-36-16-1	External 3.6V, 1600 mAH battery with plug-in connector
CBL-SET-373-G-MIN	Minimal Cable set for PCM-VDX-2-512 includes:
CBL-174-G-1-1.5	18-in., 8-wire power cable
CBL-247-G-1-1.0	1-ft., Multi-I/O adapter
BAT-LTC-E-36-16-1	External 3.6V, 1600 mAH battery with plug-in connector
Additional Cables	
CBL-174-G-1-1.5	18-in., 8-wire Power Cable
CBL-343-G-1-1.375	PS/2 Mouse Adapter
CBL-247-G-1-1.0	1-ft., Multi-I/O adapter
CBL-266-G-2-0.75	44-pin, IDE Socket Cable
CBL-DIO16-000-14	DIO Cable - Unterminated Cable
CBL-DIO16-001-12	DIO Cable with 2x_15-pin with Pico-Clasp™ connector
CBL-DIO16-002-12	DIO Cable with 2x_15-pin 0.100 center keyed female connector
CBL-ENET1-202-12	Ethernet Cable with RJ-45 Jack
CBL-ENET1-203-12	Ethernet Cable with RJ-45 Plug
CBL-SER1-202-12	Serial I/O Cable (COM3/COM4)
CBL-USB4-000-14	4x USB ports - Unterminated
CBL-USB4-001-12	4x USB ports two, 2x20-pin Pico-Clasp™ connector
CBL-USB4-002-12	4x USB ports to two, 2-mm 2x4 connectors

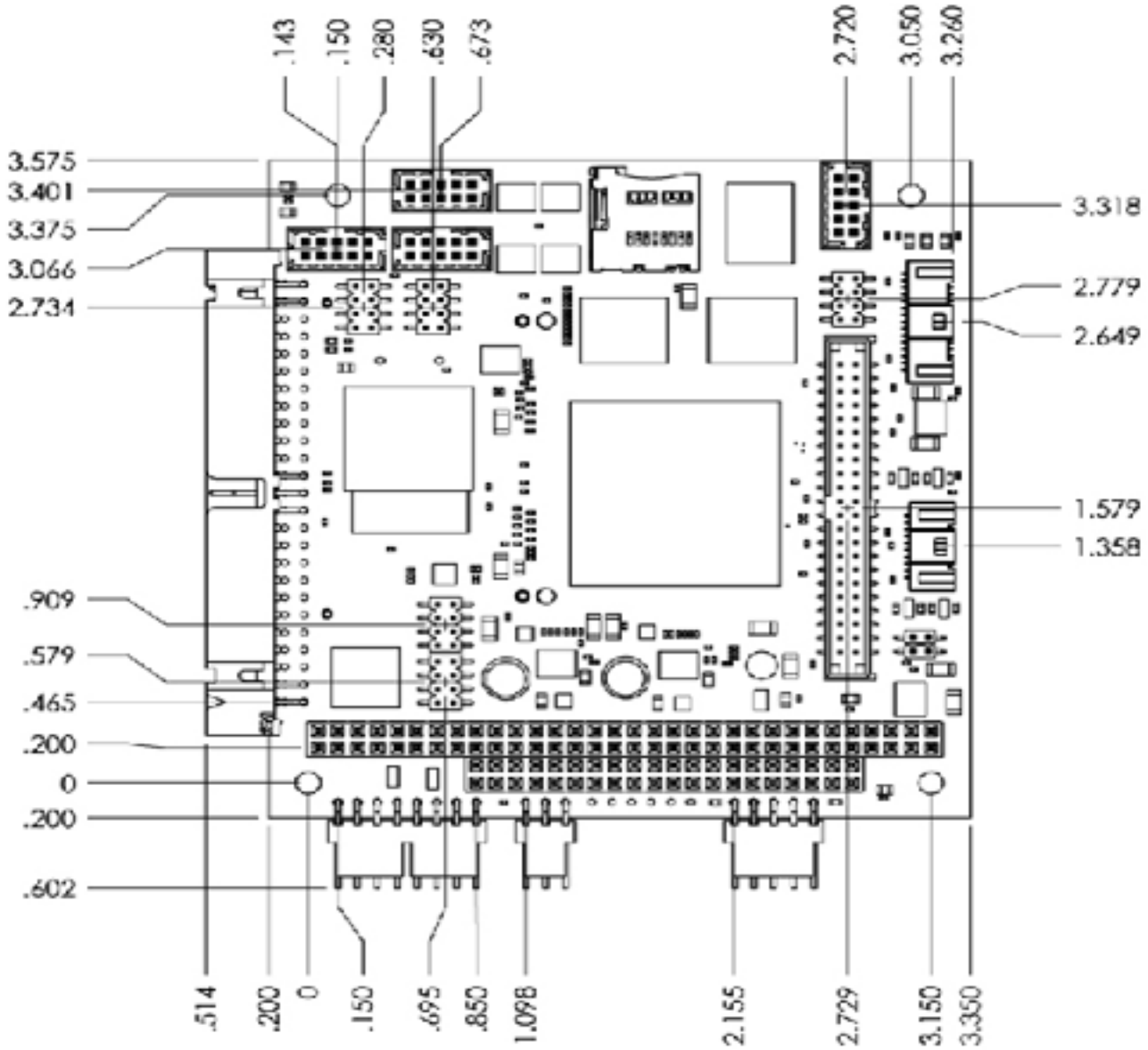
SOFTWARE DRIVERS

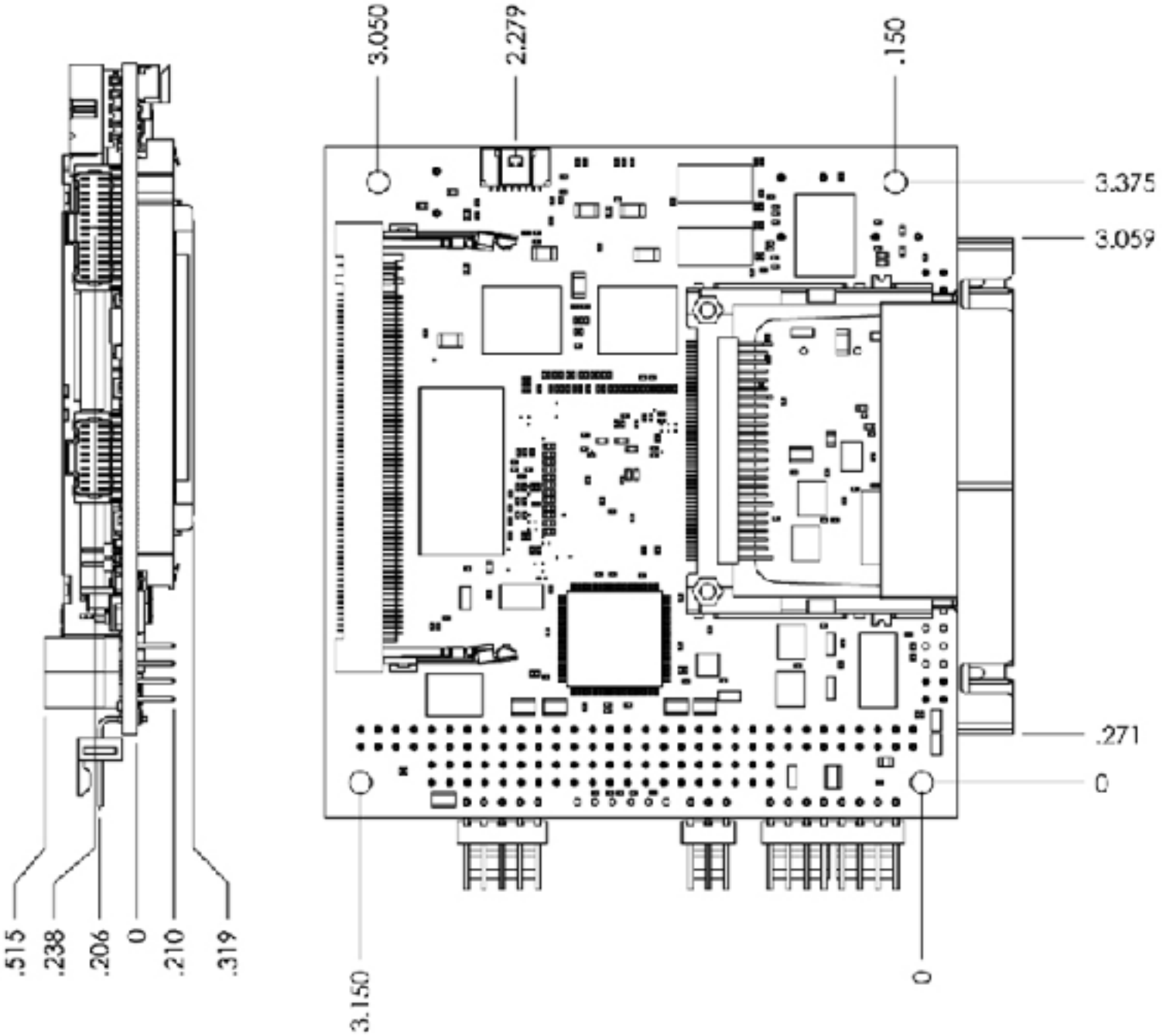
See the **WinSystems website**.

SPECIFICATIONS

Electrical		
VCC	+5VDC ±5%	
	Typical	1.2A
MTBF	11.9 years	
Mechanical		
Dimensions	3.6” x 3.8” (90 mm x 96 mm)	
Weight	3.6 oz (102g)	
Environmental		
Operating Temperature	-40°C to 85°C	

MECHANICAL DRAWING




3.050
2.279
.150
3.375
3.059
.271
0
3.150
0
.515
.238
.206
0
.210
.319

APPENDIX - A

BEST PRACTICES

POWER SUPPLY

The power supply and how it is connected to the Single Board Computer (SBC) is very important.

Avoid Electrostatic Discharge (ESD)
Only handle the SBC and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Supply Budget
Evaluate your power supply budget. It is usually good practice to budget 2X the typical power requirement for all of your devices.

Zero-Load Power Supply
Use a zero-load power supply whenever possible. A zero-load power supply does not require a minimum power load to regulate. If a zero-load power supply is not appropriate for your application, then verify that the single board computer's typical load is not lower than the power supply's minimum load. If the single board computer does not draw enough power to meet the power supply's minimum load, then the power supply will not regulate properly and can cause damage to the SBC.

Use Proper Power Connections (Voltage)
When verifying the voltage, you should always measure it at the power connector on the SBC. Measuring at the power supply does not account for voltage drop through the wire and connectors.

The single board computer requires +5V (±5%) to operate. Verify the power connections. Incorrect voltages can cause catastrophic damage.

Populate all of the +5V and ground connections. Most single board computers will have multiple power and ground pins, and all of them should be populated. The more copper connecting the power supply to the single board computer the better.

Adjusting Voltage
If you have a power supply that will allow you to adjust the voltage, it is a good idea to set the voltage at the power connector of the SBC to 5.1V. The SBC can tolerate up to 5.25V, so setting your power supply to provide 5.1V is safe and allows for a small amount of voltage drop that will occur over time as the power supply ages and the connector contacts oxidize.

Power Harness
Minimize the length of the power harness. This will reduce the amount of voltage drop between the power supply and the single board computer.

Gauge Wire
Use the largest gauge wire that you can. Most connector manufacturers have a maximum gauge wire they recommend for their pins. Try going one size larger; it usually works and the extra copper will help your system perform properly over time.

Contact Points
WinSystems' boards mostly use connectors with gold finish contacts. Gold finish contacts are used exclusively on high speed connections. Power and lower speed peripheral connectors may use a tin finish as an alternative contact surface. It is critical that the contact material in the mating connectors is matched properly (gold to gold and tin to tin). Contact areas made with dissimilar metals can cause oxidation/corrosion resulting in unreliable connections.

Pin Contacts
Often the pin contacts used in cabling are not given enough attention. The ideal choice for a pin contact would include a design similar to Molex's or Trifurcons' design, which provides three distinct points to maximize the contact area and improve connection integrity in high shock and vibration applications.

POWER DOWN

Make sure the system is **completely off/powered down** before connecting anything.

Power Supply OFF
The power supply should always be off before it is connected to the single board computer.

I/O Connections OFF
I/O Connections should also be off before connecting them to the single board computer or any I/O cards. Connecting hot signals can cause damage whether the single board computer is powered or not.

MOUNTING AND PROTECTING THE SINGLE BOARD COMPUTER

Do Not Bend or Flex the SBC
Never bend or flex the single board computer. Bending or flexing can cause irreparable damage. Single board computers are especially sensitive to flexing or bending around Ball-Grid-Array (BGA) devices. BGA devices are extremely rigid by design and flexing or bending the single board computer can cause the BGA to tear away from the printed circuit board.

Mounting Holes
The mounting holes are plated on the top, bottom and through the barrel of the hole and are connected to the single board computer's ground plane. Traces are often routed in the inner layers right below, above or around the mounting holes.

Never use a drill or any other tool in an attempt to make the holes larger.

Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.

Never use self-tapping screws; they will compromise the walls of the mounting hole.

Never use oversized screws that cut into the walls of the mounting holes.

Always use all of the mounting holes. By using all of the mounting holes you will provide the support the single board computer needs to prevent bending or flexing.

Plug or Unplug Connectors Only on Fully Mounted Boards
Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit rather tightly and the force needed to plug or unplug them could cause the single board computer to be flexed.

Avoid cutting of the SBC
Never use star washers or any fastening hardware that will cut into the single board computer.

Avoid Overtightening of Mounting Hardware
Causing the area around the mounting holes to compress could damage interlayer traces around the mouting holes.

Use Appropriate Tools
Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Placing the SBC on Mounting Standoffs
Be careful when placing the single board computer on the mounting standoffs. Sliding the board around until the standoffs are visible from the top can cause component damage on the bottom of the single board computer.

Avoid Conductive Surfaces
Never allow the single board computer to be placed on a conductive surface. Almost all single board computers use a battery to backup the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

ADDING PC/104 BOARDS TO YOUR STACK

Be careful when adding PC/104 boards to your stack.

Never allow the power to be turned on when a PC/104 board has been improperly plugged onto the stack. It is possible to misalign the PC/104 card and leave a row of pins on the end or down the long side hanging out of the connector. If power is applied with these pins misaligned, it will cause the I/O board to be damaged beyond repair.

OPERATIONS / PRODUCT MANUALS

Every single board computer has an Operations manual or Product manual.

Manual Updates
Operations/Product manuals are updated often. Periodicially check the WinSystems website (http://www.winsystems.com) for revisions.

Check Pinouts
Always check the pinout and connector locations in the manual before plugging in a cable. Many single board computers will have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

Contact an Applications Engineer with questions
If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact your Applications Engineer.

WARRANTY INFORMATION

(http://www.winsystems.com/warranty.cfm)

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WARRANTY SERVICE

1. To obtain service under this warranty, obtain a return authorization number. In the United States, contact the WinSystems' Service Center for a return authorization number. Outside the United States, contact your local sales agent for a return authorization number.

2. You must send the product postage prepaid and insured. You must enclose the products in an anti-static bag to protect from damage by static electricity. WinSystems is not responsible for damage to the product due to static electricity.